

QS6400

Datasheets

64 Poly ADPCM Sound Synthesizer For Mobile Phone.

Version 2.0

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Chapter 1 General Description

QS6400 is a high quality sound DSP for mobile phones that plays music through a built-in ADPCM decoder with sound font rom.

QS6400 is equipped with HWASS's QPCM synthesizer, which is capable of generating up to 64 voices with different tones.

QS6400 can also play two channel wavefiles of differing sampling rates.

Since data in the FIFO buffer is processed on demand, the length of the data(MIDI & WAVE) is not limited, making QS6400 an excellent platform for applications such as incoming melody distribution service.

The MIDI handler built in to QS6400 can play MIDI data without an extra buffer.

Included is a PWM module for audio out with a maximum output of 400mw at 8Ω load resistance(PVDD=4.0V)

For earphone use, QS6400 provides a single-ended stereophonic output terminal.

To operate QS6400 to full capability, "Standard MIDI File(SMF) Format 0" is recommended.

Chapter 2 Features

ADPCM synthesizer functions

- ▶ 64 voices generated at 39kHz simultaneously.
- ▶ Compatible with stereophonic sound generation.
- ▶ Master Volume control
Individual channel volume / master volume.
- ▶ Built-in MIDI handler(sequencer)
- ▶ Equipped with two buffers of 128 bytes FIFO for MIDI play.
- ▶ Built-in 4 bit or 8 bit ADPCM decoder.

TONE

- ▶ Supports GENERAL MIDI LITE specification.
GM 128 voices + 47 voices percussion.
Support to control parameters by "BxH xxh"(see the MIDI implementation chart)
- ▶ Additional 8 timbres to play korean traditional music.
Gayagum/Daegum/Heagum/Teapyoungso/Buk/Ggangary/Jangu/Jing.
- ▶ Various sampling rate : 8 ~ 39Khz

WAVE

- ▶ Support to playback ADPCM wavefile(2 Channels)
- ▶ Separate wave volume control(0-255)

CPU INTERFACING

- ▶ 1 Wire serial or 14 Wires parallel interfacing can be selected.



AUDIO OUTPUT

- ▶ PWM or 16bit DAC output can be selected.
- ▶ PWM output mode : 400mW when PVDD=4.0V, $R_L=8\Omega$
- ▶ Provides Stereo or Mono output for earphone.

POWER SUPPLY

- ▶ Includes three power supplies for sub-system
 - PVDD power supply devoted to PWM block.(3.3 ~ 4.2V)
 - EVDD power supply devoted to earphone block.(2.7 ~ 3.6V)
 - VDD is normal power supply.(2.7 ~ 3.6V)



3-2. Description of Blocks

Explanations about each block of QS6400 and flows of the signal are as follows.

1) Register Block : QS6400 has registers of 32 x 8 for storing control data.

Built-in 8052 can communicate directly with the register blocks, which are used to change control values and communicate commands. 23 x 8 registers are used for this purpose. The extra registers are available to support additional features.

2) SMF FIFO buffer : This FIFO is used in receiving SMF file blocks (128bytes) from Host.

SMF FIFO Buffer has two banks of memory block and each buffer is filled with data according to REG_IREQ_TYPE (When bit 2 is "1") from built- in 8052. When receiving a data request (IRQB) for the next procedure you should read the interrupt request type register (REG_IREQ_TYPE) to check which data is required.

3) WAVE FIFO buffer : This FIFO is used in receiving wave data blocks (64 or 128 bytes)

from Host. WAVE FIFO Buffer has four banks of memory block, of 64 bytes each. The buffer size is determined by user specification (using REG_WAVE_CHAN). Each bank is filled with wave data according to REG_IREQ_TYPE(when bit 1 or bit 0 is "1" If you intend to play high-sampling-rate(up to 22khz) wave files, we recommend that you use only one wave channel, due to the high transmission rate of data. In this case, WAVE FIFO Buffer size is preset to 128bytes.

4) Power control : This block is in charge of power management.

You can select whether to enter or wake-up from power down mode.

5) Clock generator : This block is a clock generator for the internal master clock.

QS6400 need the external clock input to operate normally.

6) CPU & ROM : This block describes 8052 micom and 12k bytes program ROM memory.

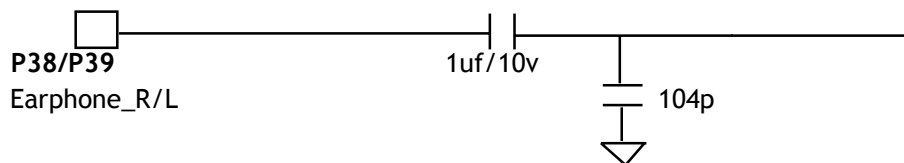
Built-in 8052 interprets SMF and Wave file.

7) PWM Speaker out : This block converts audio data into PWM format.

It supports stereophonic audio out. You can also make this output muted.

8) Earphone out : This block converts audio data into single-ended earphone signal.

You should connect poled-capacitor and bypass capacitor.





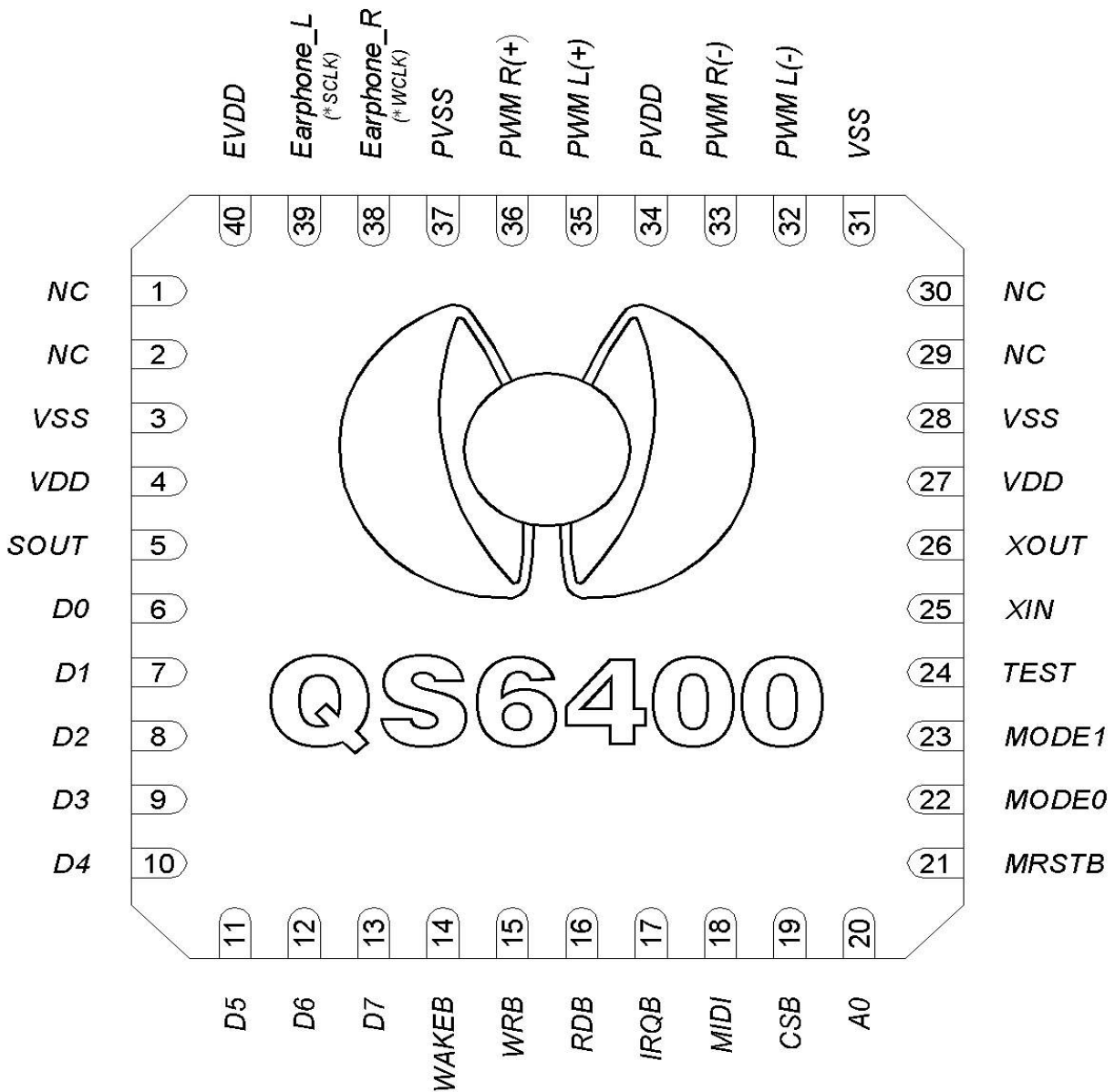
- 9) **D/A interface** : This block generates 16bit DAC interfacing out for high quality sound.
If you have an additonal DAC, you can also use this interfacing out.
When you use the DAC OUT mode, earphone out mode is disabled.

- 10) **Sound font** : This is an embedded maskrom for GM 128 sound map and 47 percussion.
The sound font built in this device stores the sampling data according to GM 128 sound map.
Additionally QS6400 has sampling data to support korean traditional music.



Chapter 4 Pin Rotation and Descriptions.

4-1. Pin Rotation





4-2. Pin Descriptions

PIN NO	PIN NAME	I/O	DESCRIPTION
1	NC	X	No Connect
2	NC	X	No Connect
3	VSS	P	Ground
4	VDD	P	Power Supply
5	SOUT	O	Serial Data Out for DAC
6	D0	I/O	Bidirection DATA BUS
7	D1	I/O	Bidirection DATA BUS
8	D2	I/O	Bidirection DATA BUS
9	D3	I/O	Bidirection DATA BUS
10	D4	I/O	Bidirection DATA BUS
11	D5	I/O	Bidirection DATA BUS
12	D6	I/O	Bidirection DATA BUS
13	D7	I/O	Bidirection DATA BUS
14	WAKEB	I	WakeUp Signal(Active Low)
15	WRB	I	Write Enable
16	RDB	I	Read Enable
17	IRQB	O	Request Data Block(Active Low)
18	MIDI	I	MIDI IN (UART)
19	CSB	I	Chip Select
20	A0	I	Register Address or Data Strobe
21	MRSTB	I	Master Reset (Active Low)
22	MODE0	I/O	LED control port or test mode
23	MODE1	I/O	Vibrator control port or test mode
24	TEST	I	Test Mode Select(must be Low)
25	XIN	I	Master Clock In
26	XOUT	I	MODE0 and MODE1 I/O select
27	VDD	P	Power Supply
28	VSS	P	Ground
29	NC	X	No Connect
30	NC	X	No Connect
31	VSS	P	Ground
32	PWML(-)	O	PWM Output Left (-)
33	PWMR(-)	O	PWM Output Right (-)
34	PVDD	I	PWM Power
35	PWML(+)	O	PWM Output Left (+)
36	PWMR(+)	O	PWM Output Right (+)
37	PVSS	I	PWM Ground
38	EarPhone_R(*Wclk)	O	EarPhone out Right or Word Clock for DAC
39	EarPhone_L(*Sclk)	O	EarPhone out Left or Serial Clock for DAC
40	EVDD	P	Power for EarPhone



4-3. Detail pin descriptions.

▶ POWER SUPPLY PINS

- VDD (4,27)

These pins are connected to a normal power supplier.

- VSS (3,28,31)

These pins are GNDs of power.

- PVDD(34), EVDD(40),PVSS (37)

PVDD is VDD for PWM block. It's capable of driving a voltage of MAX 4.2V down to 3.3V.

EVDD is VDD for EarPhone block. Its range covers 3.6V to 2.7V.

PVSS is PWM block GND.

▶ POWER RESET

- MRSTB (21)

Reset is accomplished by holding the MRSTB pin low for at least 60 oscillator periods while the oscillator is running. To ensure proper power-on reset, the MRSTB pin must be high long enough to allow the oscillator time to start up plus 40 oscillator periods.

RESET plus should be free from glitch noise.

At power-on, the voltage on VDD and MRSTB must come up at the same time for a proper start-up.

After RESET, all registers and internal RAM are initialized to "0x00".

▶ AUDIO INTERFACE

QS6400 supports two kinds of output mode; DAC out or PWM out

There is a register for selecting output mode.

In using PWM mode, you can select Stereo or Mono out. Thus QS6400 can support application such as high-quality stereo mobile phones.

QS6400 also provides single-ended stereophonic earphone output, showing superb playback quality through both External speakers and earphones.

You can select these modes using REG_OUT_MODE.

- PWML-(32), PWML+(35), PWMR-(33),PWMR+(36)

QS6400 supports Stereo PWM out for the Speaker. This output can be muted if desired.

PWML- and PWMR- are connected to the speaker's minus(-) terminal.

PWML+ and PWMR+ should be connected to the plus(+) terminal.

- EarPhone_R(38), EarPhone_L(39)

EarPhone_R and EarPhone_L are single- Ended Stereo EarPhone output modes.

EVDD is prepared to power earphone operation separately.

Also you can mute PWM output signal by control bit located in REG_OUT_MODE.

- WCLK (*38), SCLK (*39), SOUT (5)

If you write data "1xxxxxxH" to "(Out_Mode)" after reset, DAC mode is enabled and Earphone out is disabled.

On the other hand, if you need EarPhone out mode, you can choose EarPhone out Mode.

If you want more detailed information, see "Chapter 5-3 D/A interface and Chapter 5-4 Earphone out".



▶ CPU INTERFACE

QS6400 provides 1 wire serial interface and 14 wires parallel interface. These are processed at the same time without extra control commands.

□ MIDI (18)

Interface for serial MIDI signal. The input signal should be of asynchronous serial type with no-parity bit and should have one start and stop bit each, thus consisting of ten total bits. The transfer mode should be MSB first method.

□ IRQB (17)

Request pin(IRQB) that is activated when QS6400 is ready to receive next packet data block. After receiving this request, you must read the interrupt request type register(REG_IREQ_TYPE) which you want. At this time IRQB is cleared.

To play MIDI file you should transfer 128 byte data blocks.

To play wave files, you should transfer 64 or 128 bytes of data.

You can select the data block size by write value to wave channel number register(REG_WAVE_CN)

If you take one wave channel, data block size is 128 bytes.

If you want to play two wavfiles simultaneously. the data block should be $128/2 = 64$ bytes.

□ WAKEB (14)

WAKEB is to release from Power-Down Mode. A wake operation is accomplished by holding the WAKEB pin low for a minimum of 70ns period.

After wakeup, all internal registers and RAM buffers are initialized to zero.

□ A0(20)

This pin is used to select between Register Address or Command and Data. If the pin is high, the data to be written is the Register Address(Index) . Otherwise if the pin is low, the data to be written is Command or Data.

□ CSB(19)

Chip Select for QS6400. This pin must be low for read and write operation.

□ D0-D7(6-13)

These are data buses for INDEX and DATA.

We recommend use of COMMON DATA BUS.

▶ EXTRA PINS

□ XIN (25)

□ XOUT (26)

This pin determines I/O status of MODE0 and MODE1. When High, MODE0 and MODE1 are set to input mode. However, in this case either one of MODE0 or MODE1 must be High.

If both are Low, that signals a self diagnostic mode.

When XOUT is Low, MODE0 and MODE1 are used in output mode, with MODE0 and MODE1 each controlling the LED and the Vibrator, respectively.



Chapter 5 Details of Blocks.

5-1. REGISTER

5-1-1. REGISTER TABLE

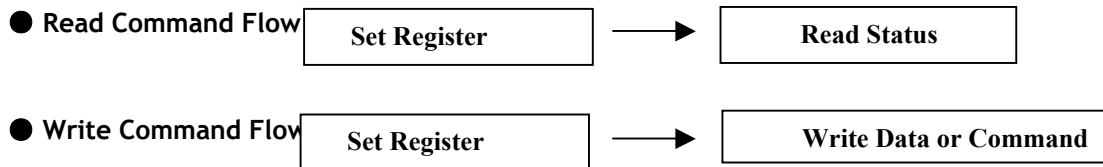
Registers	Address	R/W	Description
RESERVED	00H	X	Reserved
RESERVED	01H	X	Reserved
RESERVED	02H	X	Reserved
REG_SMF_CTRL	03H	W	SMF play control register (play/stop/etc.)
REG_VOLUME	04H	W	PWMR and PWML gain control register
REG_SMF_EOP	05H	W	End of a packet(128 bytes) register for the SMF
REG_PIO_MIDI	06H	W	Parallel MIDI interface register
REG_WAVE_CHAN	07H	W	Register to specify number of wave channels to use
REG_WAV1_CTRL	08H	W	Wave channel 1 play control register
REG_WAV_VOL	09H	W	Wave volume control register
REG_PTR_FIFO	0AH	W	Pointer register of the SMF fifo for single midi mode
REG_WAV1_SR	0BH	W	Wave channel 1 sample rate select register
REG_WAV2_CTRL	0CH	W	Wave channel 2 play control register
REG_LED_MODE	0DH	W	LED mode select register
REG_VIB_MODE	0EH	W	Vibrator mode select register
REG_WAV2_SR	0FH	W	wave channel 2 sample rate select register
REG_LV_CTRL	10H	W	Led and vibrator on/off control register
REG_SMF_BUF	11H	W	SMF packet block buffer register (128bytes)
REG_WAV1_BUF	12H	W	Wave channel 1 packet block buffer register
REG_WAV2_BUF	13H	W	Wave channel 2 packet block buffer register
REG_READY_QS	14H	W	Ready for active of QS6400
REG_REF_TUNE	15H	W	Reference Clock Select
REG_OUT_MODE	16H	W	Audio output mode select register
REG_P_DOWN	17H	W	Power down mode register
REG_EARP_VOL	18H	W	Earphone volume control register
REG_PWM_CLOCK	19H	W	PWM Clock Rate Selector
REG_IREQ_TYPE	1AH	R	Interrupt request type register(Read only)
RESERVED	1BH	X	Reserved
REG_QDSP_MODE	1CH	R	Status bit for SMF & WAVE Channel.(Read only)
READ_WRITE_BACK	1DH	R	Read the INDEX to be written before (Read only)
RESERVED	1EH	X	Reserved
RESERVED	1FH	X	Reserved
RESERVED	20H	X	Reserved
RESERVED	21H	X	Reserved
REG_IF_FLAG1	22H	R	Flag1 register to notify 8-registers writing state
REG_IF_FLAG2	23H	R	Flag2 register to notify 8-registers writing state
REG_IF_FLAG3	24H	R	Flag3 register to notify 8-registers writing state
REG_IF_FLAG4	25H	R	Flag4 register to notify 8-registers writing state



5-1-2. READ AND WRITE OPERATION

	WRB	RDB	A0	CSB	D0 -D7
Set Address	↑	H	H	L	Set register address to write or read
Read Register	H	↑	L	L	Read data from QS6400
Write Register	↑	H	L	L	Write command to QS6400

To write Data or a Command to a register, first set A0 to High and CSB to low. After writing the Index Address of target register, set both A0 and CSB to low to write command or data.



5-1-3. DETAILED REGISTER DESCRIPTIONS AND USEAGES IN EACH ACTION

▶ INITIAL SETUP WHEN POWER ON RESET.

1) RELATED TO DEVICE READY CHECK BETWEEN HOST AND QS6400

□ REG_READY_QS : 0x14

Data	Description
0x4D	Ready command for ACTION of QS6400

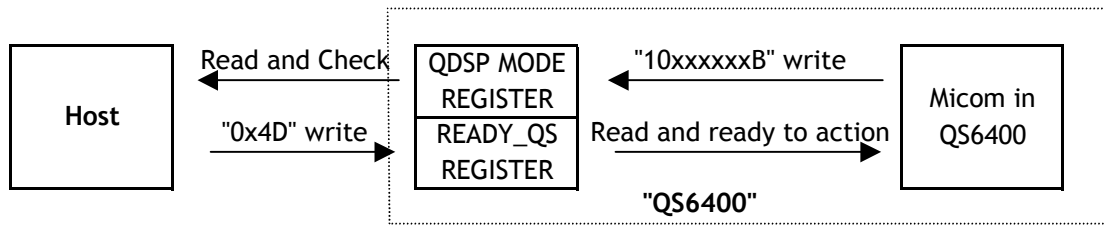
This register relays an initialization signal to the QS6400. For normal initialization write "0x4D".

*Warning => This register is also used to test the operation of the chip, and any other value should not be written to it

□ REG_QDSP_MODE : 0x1C

Internal operation status of QS6400

Bit	Mode	Description
Bit 0	H	Ready Wave Channel #1
	L	Busy Wave Channel #1
Bit 1	H	Ready Wave Channel #2
	L	Busy Wave Channel #2
Bit 2	H	fade out complete mode by power down
	L	normal mode
Bit 3	H	midi file play mode
	L	midi file stop mode
Bit 4	H	not used
	L	reserved
Bit 5	H	single MIDI protocol FIFO mode
	L	normal FIFO using mode
Bit 6	H	abnormal wake up mode
	L	normal wake up mode
Bit 7	H	normal wake up mode
	L	abnormal wake up mode



2) RELATED TO QS6400 INITIAL VALUE

□ REG_VOLUME : 0x04

DATA	Description
0x00 - 0xFF	PWMR and PWML gain control

This register adjusts the output gain on Speaker driven by internal amplifier of QS6400. Valid range is 0-255. User sets this value according to desired output.

□ REG_WAVE_CHAN : 0x07

DATA	Description
0x00	Do not use any Wave(ADPCM) decoder channels.
0x01	Use one Wave(ADPCM) decoder channel. On request of Wave Data Packet, 128 bytes must be transferred.
0x02	Use two Wave(ADPCM) decoder channels. On request of Wave Data Packet, 64 bytes must be transferred.

The number of ADPCM decoder channels to be used during ADPCM wave file playback is decided by this register. The internal Wave FIFO buffer is utilized differently depending on this value.

□ REG_WAV_VOL : 0x09

DATA	Description
0x00 - 0xFF	Set Wave Play Volume for Wave Channels

Sets the volume of the ADPCM decoder. Range is 0-255.

□ REG_EARP_VOL : 0x18

Bit7	Description
1	Earphone Out Left Volume. Range : 0 ~ 127(Bit6 ~ Bit0)
0	Earphone Out Right Volume. Range : 0 ~ 127(Bit6 ~ Bit0)

This register sets earphone out volume.

□ REG_PWM_CLOCK : 0x19

DATA	Description
0x00	40Mhz for PWM drive clock
0x01	20Mhz for PWM drive clock

Register to select internal clock mode to drive PWM.



3) AUDIO OUT SELECT REGISTER

□ REG_OUT_MODE : 0x16

DATA	Description	
Bit 7	L	Select PWM for Audio out
	H	Select DAC for Audio out
Bit 6	L	Set PWM out Enable
	H	Set PWM out Disable(Mute)
Bit 5	L	Undefined
	H	Undefined
Bit 4	L	Set Stereo Mode
	H	Set Mono Mode
Bit 3	L	Undefined
	H	Undefined
Bit 2	L	Earphone Right Out Enable
	H	Earphone Right Out Disable(Mute)
Bit 1	L	Earphone Left Out Enable
	H	Earphone Left Out Disable(Mute)
Bit 0	x	Undefined

Sets stereo/mono mode of Audio out and also enables/disables mute for each output signal.

4) REFERENCE CLOCK SELECT REGISTER

□ REG_REF_TUNE : 0x15

This register is used to correct the internal clock that is generated in tandem to the external reference clock. It has to be set to the correct value according to the clock frequency received on Xin. A disparage between the frequency of clock value set in this register and Xin will result in sounds of abnormal pitch and tempo.

Values for each frequency are as follows:

DATA	Xin Reference Clock
0	Reference Clock = 13Mhz
1	Reference Clock = 19.2Mhz
2	Reference Clock = 26Mhz
3	Reference Clock = 24Mhz
4	Reference Clock = 13Mhz
5	Reference Clock = 19.2Mhz
6	Reference Clock = 26Mhz
7	Reference Clock = 24Mhz
8	Reference Clock = 13Mhz
9	Reference Clock = 19.68Mhz
10	Reference Clock = 26Mhz
11	Reference Clock = 24Mhz
12	Reference Clock = 13Mhz
13	Reference Clock = 19.68Mhz
14	Reference Clock = 26Mhz
15	Reference Clock = 24Mhz



16 ~ 255	<p>Reference Clock = Register Value / 10</p> <p>ex) Register Value = 16, Reference Clock = 1.6Mhz Register Value = 21, Reference Clock = 2.1Mhz Register Value = 96, Reference Clock = 9.6Mhz</p>
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▶ RELATED TO PLAY MIDI REGISTER

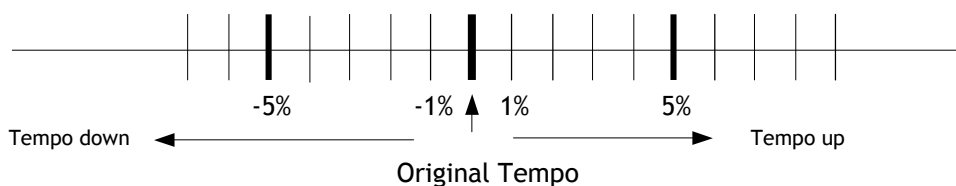
□ REG_SMF_CTRL : 0x03

This register controls Standard MIDI File(SMF) playback.

Operations are decided by bits written to this register.

Function	Data	Description
Playback	0x11	Starts play of SMF.
	0x12	Stops play of SMF.
	0x13	Pauses play of SMF. Should only be used during playback.
	0x14	Resumes play of SMF from pause state. Should only be used when paused.
Tempo	0x20	Sets Tempo to base tempo, removing any changes that have been made to the Tempo.
	0x21	Tempo increases in steps of 1% against base tempo, to a maximum of 25%. (Cannot be used while playing an ADPCM Wave File)
	0x22	Tempo decreases in steps of 1% against base tempo, to a maximum of 25%. (Cannot be used while playing an ADPCM Wave File)
FIFO	0x31	Sets mode of MIDI FIFO buffer to be used as a MIDI protocol input buffer to an external MIDI sequencer. The internal sequencer of the QS6400 is disabled in this mode.
	0x32	Returns to normal mode, canceling use of the MIDI FIFO buffer as input to an external sequencer.
Key Shift	0x40	Sets key to base key, removing any changes that have been made to the key.
	0x41	Key is increased by one pitch. Can be increased by a maximum of 12.
	0x42	Key is decreased by one pitch. Can be decreased by a maximum of 12.

*Tempo step up from original tempo value. (Total 50 steps)





□ REG_SMF_BUF : 0x11

Write data to this register during SMF data packet transfer.

For a continuous write, just initiate the first write.

This can also be used as a buffer for direct external input of MIDI protocol data.

DATA	Description
SMF DATA	MIDI Packet Data Buffer Write Address(128Bytes)

After receiving the next data request, you should write the data to this address in a block of 128 bytes. And then write dummy data to "REG_SMF_EOP" register to acquire to finish this packet.

□ REG_SMF_EOP : 0x05

DATA	Description
ANY DATA	Finished MIDI data write.

This register notifies the transfer of a 128 byte data packet is completed upon request for the next SMF data packet during playback.

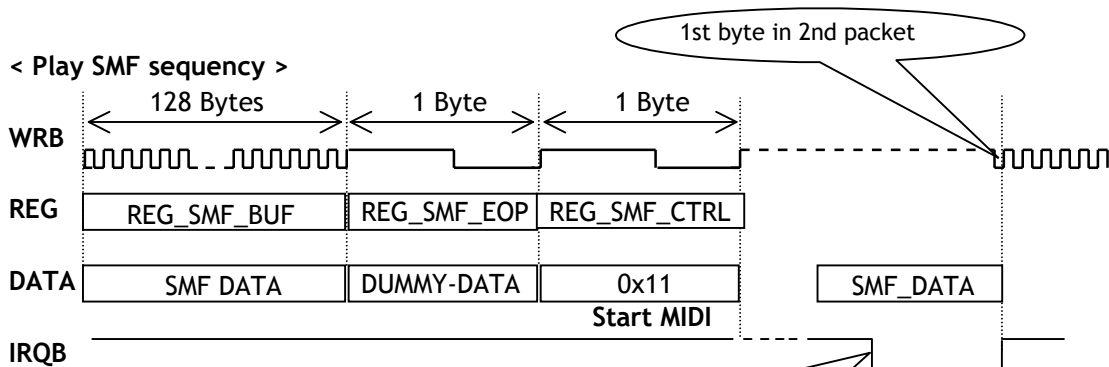
It is only used to control SMF data transfer, and is activated by any non-zero value.

□ REG_IREQ_TYPE : 0x1A

Determines which request has been made when IRQB pin is Low. Reading this register resets IRQB to High.

DATA	Description
Bit 0	On request of next data packet of Wave channel 2.
Bit 1	On request of next data packet of Wave channel 1.
Bit 2	On request for next data packet of Song File
Bit 3	Reserved
Bit 4	Reserved
Bit 5	When playback of Song File has ended
Bit 6	Start/Stop of Wave channel 2 during playback of Song File.
Bit 7	Start/Stop of Wave channel 1 during playback of Song File.

(H : request active , L : no request)



<Next data block request>
 Check the [REG_IREQ_TYPE](#) which bit 2 is "1" and then write the packet data to be required.



< Detailed register control to play the SMF file >

- STEP 1- REG_SMF_BUF(11H) <---- OxFF ; To write the 1st packet data(128bytes).
- STEP 2- REG_SMF_CTRL(03H) <---- 0x11 ; Start play of the SMF file.
- STEP 3- REG_SMF_EOP(05H) <---- OxFF ; Write the dummy data for finishing packet data transfer.
- STEP 4- Check "Data Request" ; Next packet request(IRQB) from QS6400
- STEP 5- REG_IREQ_TYPE(1AH) <---- ; Read "REG_IREQ_TYPE" and Check if bit 2 is "1"
- STEP 6- REG_SMF_BUF(11H) <---- OxFF ; To write the 2nd packet data(128bytes).
- STEP 7- REG_SMF_EOP(05H) <---- OxFF ; Write the dummy data for finishing packet data transfer.

packet data writing process

Repeat packet data writing process

"
"
"
"
"
"
"
"

Repeat packet data writing process

- STEP 8- Check "Data Request" ; Next packet request(IRQB) from QS6400
- STEP 9- REG_IREQ_TYPE(1AH) <---- ; Read "REG_IREQ_TYPE" and Check if bit 2 is "SET"
- STEP10- REG_SMF_BUF(11H) <---- OxFF ; Write the last packet data(128bytes)
- STEP11- REG_SMF_EOP(05H) <---- OxFF ; Write the dummy data for finishing packet data transfer.

Last packet

- STEP 12- Check "Data Request" ; Next packet request(IRQB) from QS6400
- STEP 13- REG_IREQ_TYPE(1AH) <---- ; Read "REG_IREQ_TYPE" and Check if bit 5 is "SET"

Stop the SMF Play



► RELATED TO PLAY WAVE REGISTER

□ REG_WAV1_CTRL : 0x08

DATA	Description
0x11	Start decode on Wave Channel 1.
0x12	Stop decode on Wave Channel 1

This controls the ADPCM decoder of the first Wave Channel.

□ REG_WAV1_SR : 0x0B

Sets type of ADPCM decoder channel 1.

Bit7 ~ Bit6	Bit5 ~ Bit4	Bit3 ~ Bit0
ADPCM table Select	Filter Select or Sub Sampling Rate Select	Sampling Rate

	Bit7	Bit6	Description
ADPCM table Select	0	0	Using ADPCM table 1 (19T)
	0	1	Using ADPCM table 2 (08T)
	1	0	Using ADPCM table 3 (04T)
	1	1	Using ADPCM table 4 (02T)

	Bit5	Bit4	Description
Filter Select or Sub Sampling Rate Select	0	0	Without Filter Mode
	0	1	Filter 1 Mode
	1	0	Filter 2 Mode
	1	1	Sub Sampling Mode

	Main Sampling Rate					Sub Sampling Rate				
Bit3 ~ Bit0	0x00	0x01	0x02	0x03	0x04	0x0A	0x0B	0x0C	0x0D	0x0E
Sampling Rate	22.1K	14.7K	11K	8.82K	4.41K	8K	7K	6K	5K	3.6K

□ REG_WAV2_CTRL : 0x0C

DATA	Description
0x11	Start decode on Wave Channel 2.
0x12	Stop decode on Wave Channel 2

This controls the ADPCM decoder of the second Wave Channel.

□ REG_WAV2_SR : 0x0F

Sets type of ADPCM decoder channel 2.

Bit7 ~ Bit6	Bit5 ~ Bit4	Bit3 ~ Bit0
ADPCM table Select	Filter Select or Sub Sampling Rate Select	Sampling Rate



	Bit7	Bit6	Description
ADPCM table Select	0	0	Using ADPCM table 1 (19T)
	0	1	Using ADPCM table 2 (08T)
	1	0	Using ADPCM table 3 (04T)
	1	1	Using ADPCM table 4 (02T)

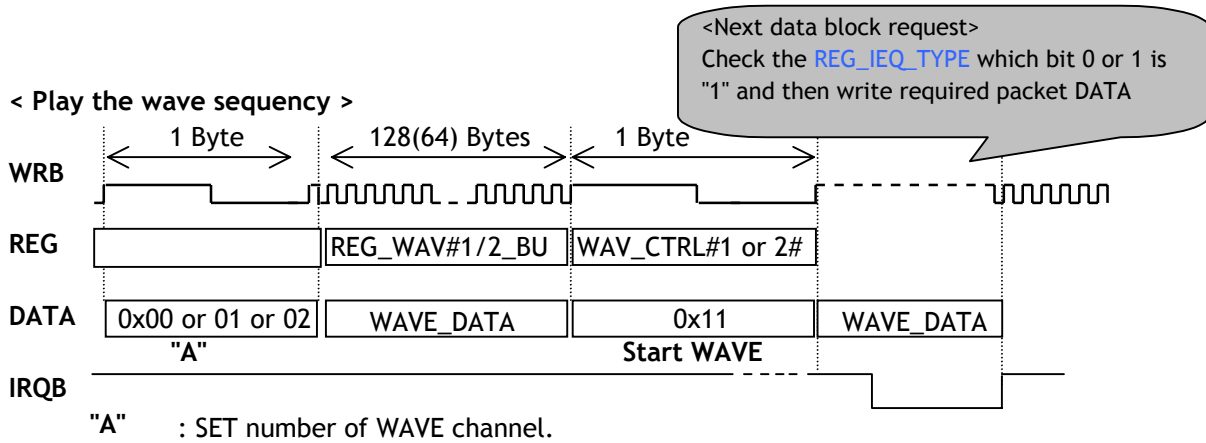
	Bit5	Bit4	Description
Filter Select or Sub Sampling Rate Select	0	0	Without Filter Mode
	0	1	Filter 1 Mode
	1	0	Filter 2 Mode
	1	1	Sub Sampling Mode

	Main Sampling Rate					Sub Sampling Rate				
Bit3 ~ Bit0	0x00	0x01	0x02	0x03	0x04	0x0A	0x0B	0x0C	0x0D	0x0E
Sampling Rate	22.1K	14.7K	11K	8.82K	4.41K	8K	7K	6K	5K	3.6K

□ REG_WAV1_BUF : 0x12 & REG_WAV2_BUF : 0x13

DATA	Description
WAVE DATA	Wave#1/2 Packet Data Buffer (**bytes)

****bytes** : If you select one-wave channel, you should write packet data of 128 byte.
If you select two-wave channel, you should write packet data of 64 byte.





< Detailed register control for playing the WAVE file "When wave channel is one" >

- STEP 1- REG_WAV_VOL(09H) <---- OxFF ; Set Wave volume
- STEP 2- REG_WAV1_SR(0BH) <---- Ox09 ; Set sampling-rate and number of data bit.
- STEP 3- REG_WAV1_BUF(12H) <---- OxFF ; Write the packet data for playing wave.(128byte)
- STEP 4- EG_WAV1_CTRL(08H) <---- Ox11 ; Start the WAVE file.
- STEP 5- Check "Data Request" ; Next packet request(IRQB) from QS6400
- STEP 6- REG_IREQ_TYPE(1AH) ; Read "REG_IREQ_TYPE" and Check if bit 1 is "SET"
- STEP 7- REG_WAV1_BUF(12H) <---- OxFF ; Write the 2nd packet data for playing wave.(128byte)

Repeat packet data writing process

''
''
''
''
''
''
''
''
''

Repeat packet data writing process

- STEP 8- Check "Data Request" ; Next packet request(IRQB) from QS6400
- STEP 9- REG_IREQ_TYPE(1AH) ; Read "REG_IREQ_TYPE" and Check if bit 1 is "SET"
- STEP10- REG_WAV1_BUF(12H) <---- OxFF ; Write the last packet data(128byte) Last packet data
- STEP11- EG_WAV1_CTRL(08H) <---- Ox12 ; STOP the WAVE play.



▶ RELATED TO ONE NOTE MIDI PLAY

□ REG_PIO_MIDI : 0x06

DATA	Description
MIDI BYTE	Support to input midi data by parallel format

This register is used for direct input of MIDI protocol by the user.
 The data is provided by the user and 0-2mSec are required for data read.
 This is useful for producing a Key Tone of a specific sound in the GM sound map.

□ REG_PTR_FIFO : 0x0A

Used to notify the QS6400 on the 256byte buffer offset Address during transfer on a by MIDI protocol data basis, using the SMF FIFO buffer.

▶ POWER MANEGEMENT REGISTER

□ REG_P_DOWN : 0x17

Puts QS6400 in power down mode.
 This is also used to stop internal clock generator adjustment.

DATA	Description
0xAA	Enters Power Down Mode
0x55	Gradually reduces currently operating Polys. (Fade Out)
0x01	Stops internal clock adjustment algorithm

▶ GPIO CONTROL REGISTER

□ REG_LED_MODE : 0x0D

Sets behavior of LED when controlled using MODE0(#22) pin.

Bit7	Bit6 ~ Bit4	Bit3 ~ Bit0
0	LED operation mode	LED blink frequency (LED_BF)

*Bit7 must be '0'. Setting to '1' signals use of register for sound test, so it must be set to '0' for

this register to be used as a control parameter.
 Bit7 = '1', Bit6 = '0': Bit5-Bit0 become internal ENV_ATTENUATE.

* LED operation Mode

Bit6	Bit5	Bit4	
0	0	0	Sync. with LED control
0	1	0	Sync. with LED control
0	1	1	Sync. with LED control + Blinking
1	1	0	Reserved Mode
1	1	1	Reserved Mode
etc			Reserved Mode

* LED blink freq.
 Blinking Frequency = 100 / (4 x LED_BF) Hz
 Will not blink if LED_BF is set to "0".



□ REG_VIB_MODE : 0x0E

Sets behavior of Vibrator when controlled using MODE1(#23) pin.

Bit7	Bit6 ~ Bit4	Bit3 ~ Bit0
0	Vibrator operation mode	Vibrator blink frequency (VIB_BF)

*Bit7 must be '0'. Setting to '1' signals use of register for sound test, so it must be set to '0' for

this register to be used as a control parameter.

Bit7 = '1', Bit6 = '0': Bit5~Bit0 become internal PD_ENV_DECAY.

* Vibrator operation Mode

Bit6	Bit5	Bit4	
0	0	0	Sync. with Vibrator control
0	1	0	Sync. with Vibrator control
0	1	1	Sync. with Vibrator control + Blinking
1	1	0	Reserved Mode
1	1	1	Reserved Mode
etc			Reserved Mode

* Vibrator blink freq.

Blinking Frequency = 100 / (4 x VIB_BF) Hz

Will not blink if VIB_BF is set to "0".

□ REG_WRITE_BACK : 0x1D

Returns Register Index Number when QS6400 reads a Command or Data that has previously been written to some register.

Used to verify that the internal processor has read some specific value that was written.



5-2. FIFO

QS6400 have two kinds of FIFO to play MIDI and WAVE DATA. These FIFOs are prepared for receiving the SMF file and Wave data from Host. Both of them have two banks of memory block and each buffer is filled with data according to REG_IREQ_TYPE from built- in 8052. They both have the same address. Address is automatically incremented during operation. When receiving the data request(IRQB) for next procedure you should read the REG_IREQ_TYPE register and then send the next data by request type.

< FIFO for MIDI >

*03H	0	1	2	3	4	5	122	123	124	125	126	127
------	---	---	---	---	---	---	------	-----	-----	-----	-----	-----	-----

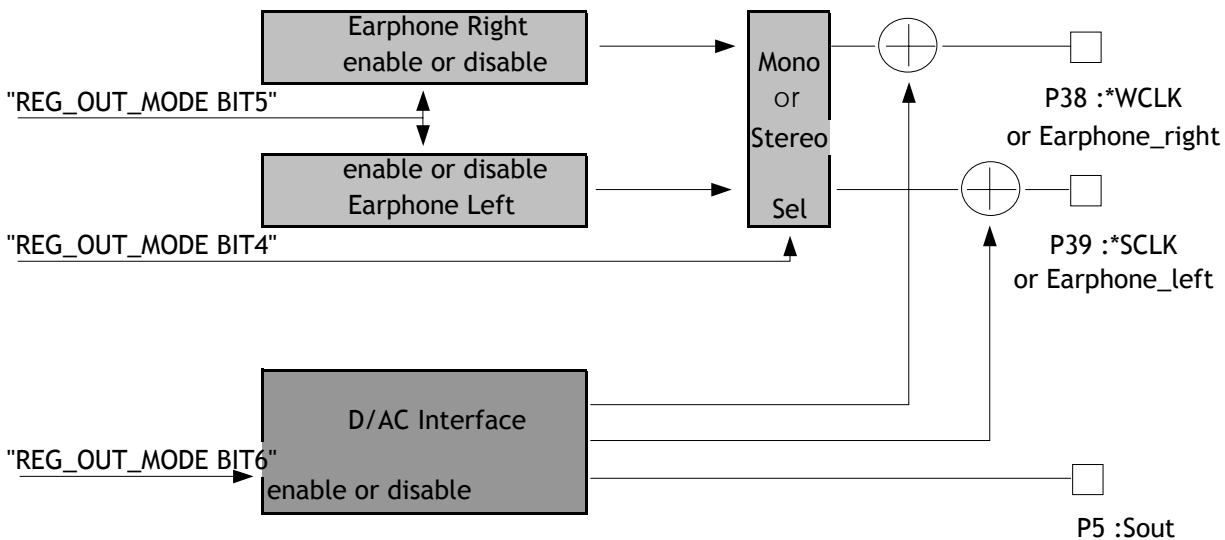
*03H	0	1	2	3	4	5	122	123	124	125	126	127
------	---	---	---	---	---	---	------	-----	-----	-----	-----	-----	-----

< FIFO for WAVE >

WAVE_CH#1	0	1	2	3	4	5	58	59	60	61	62	63
WAVE_CH#2	0	1	2	3	4	5	58	59	60	61	62	63

5-3. D/A AND EARPHONE OUTPUT

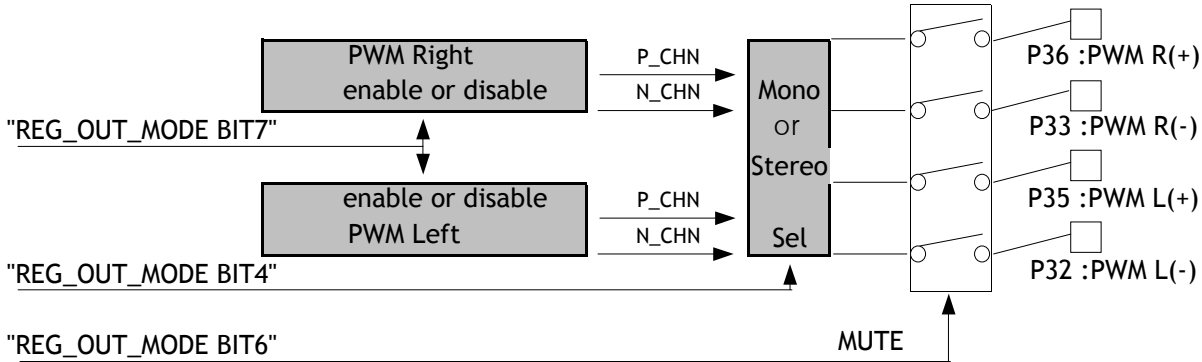
QS6400 provides switchable audio out mode between DAC and EARPHONE. Using the output-mode register you can select whether audio output is DAC or Earphone. When using earphone out, the DAC interface is in accessible, because the DAC and Earphone out pin actually use the same hardware pin.





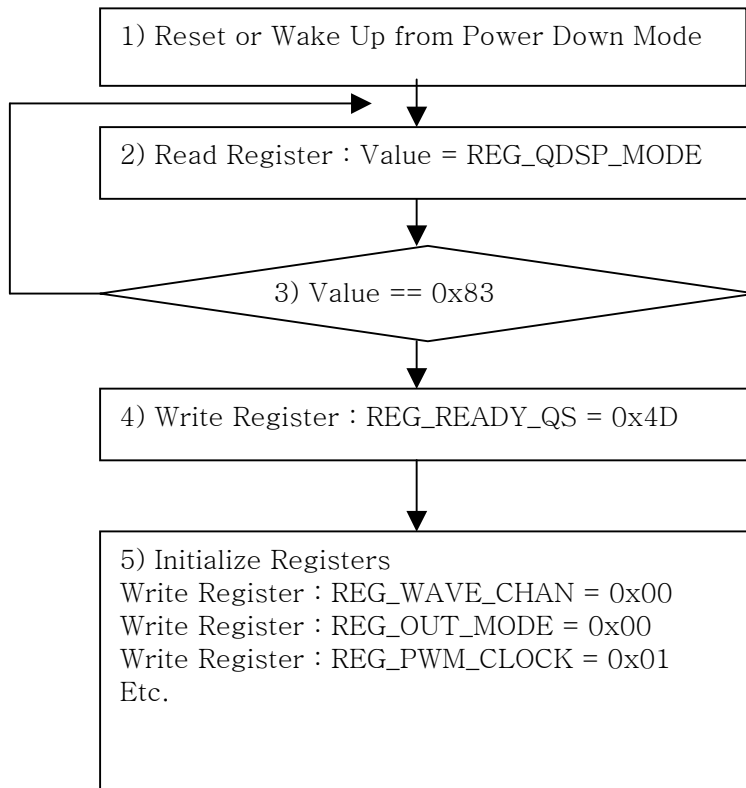
5-4. STEREO PWM OUTPUT

QS6400 supports two kinds of speaker out mode, DAC out or PWM out. In using PWM mode, you should select whether it is Stereo or Mono.



Chapter 6 Application Flow Chart

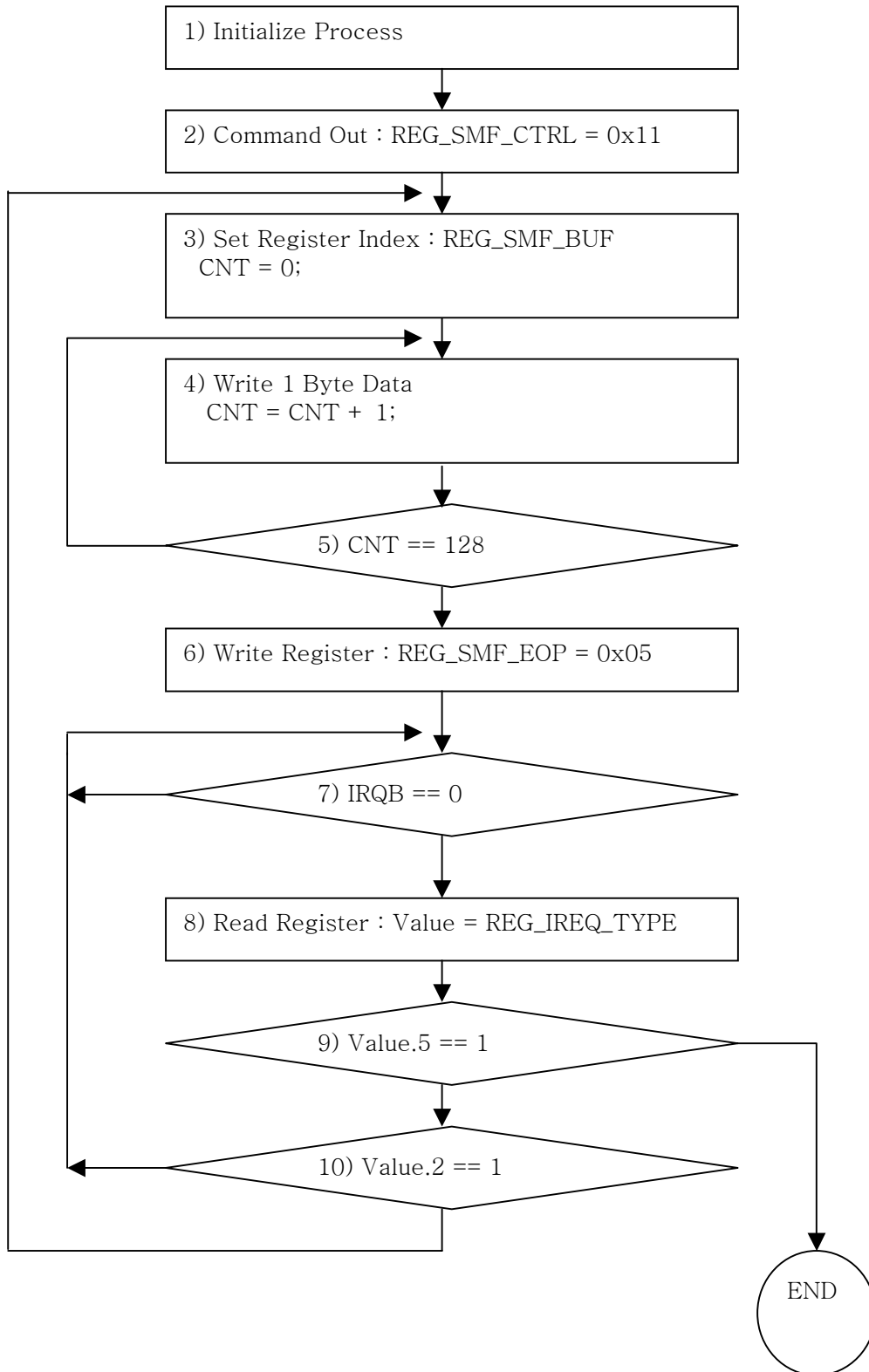
[QS6400 Initialize]



[Note] If "0x83" is not detected on step 3) for over 300mSec, regard as hardware failure in QS6400.

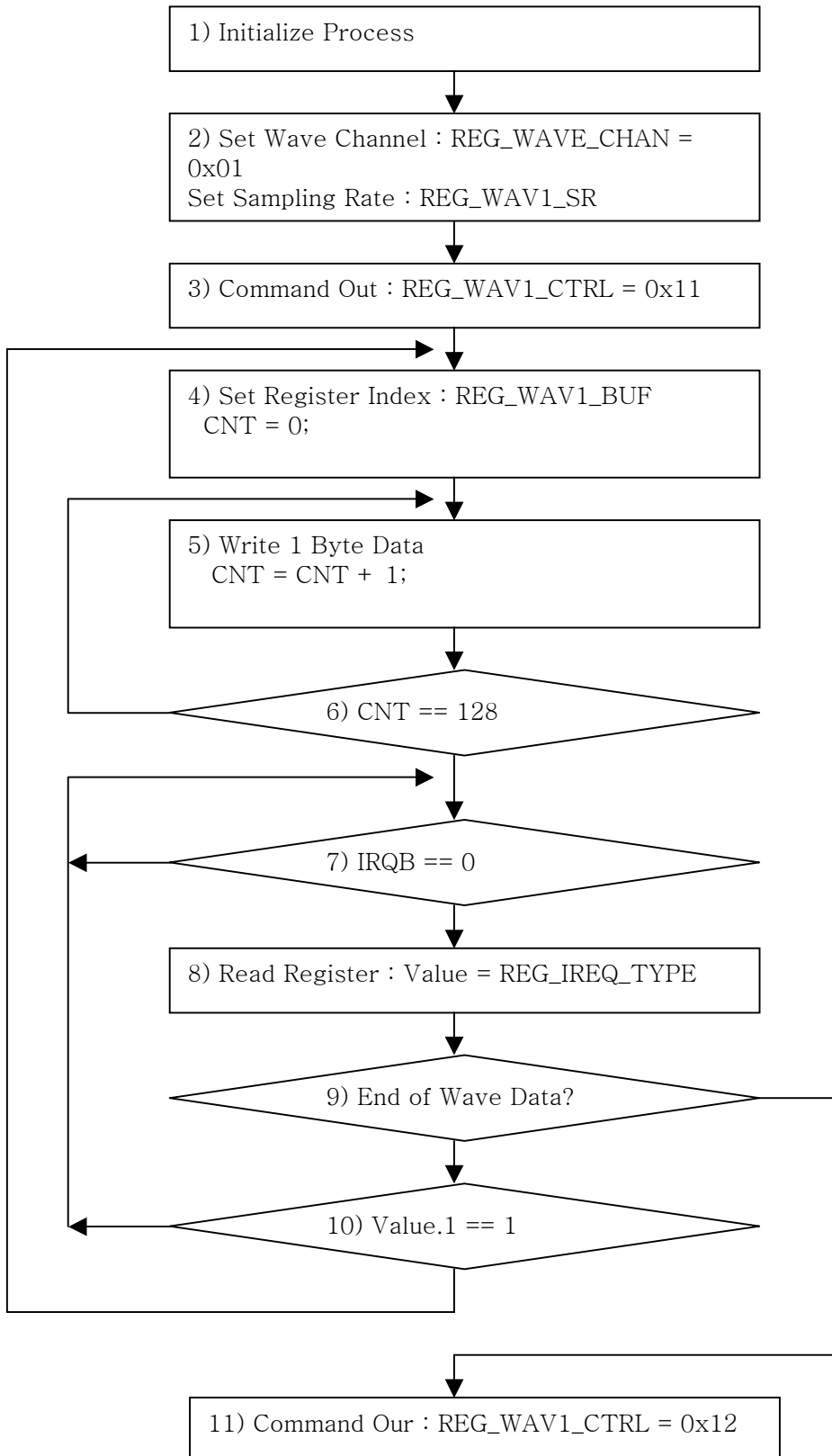


[QS6400 MIDI File Play Flow]





[QS6400 WAVE File Play Flow]





Chapter 7 Eletrical Charateristics and soldering temperature

Absolute maximum range

Item	Symbol	Min	Max	Unit
PVDD terminal power supply voltage	PVDD	-0.5	4.5	V
VDD terminal power supply voltage	VDD	-0.5	4.0	V
EVDD terminal power supply voltage	EVDD	-5	4.0	V
Digital input voltage	VIND	VSS-0.5	VDD+0.5	V
Operating ambient temperature	TOP	-20	85	deg. C
Carrier temperature	TCA	-50	125	deg. C

Recommended operating condition

Item	Symbol	Min	Typ	Max	Unit
PVDD operating voltage	PVDD	2.7	3	4.2	V
EVDD operating voltage	EVDD	2.5	3	3.6	
VDD operating voltage	VDD	2.5	3	3.6	V
Operating ambient temperature	TOP	-20	25	85	deg. C

DC characteristics

Note : VDD = 3.3V , VSS = 0V

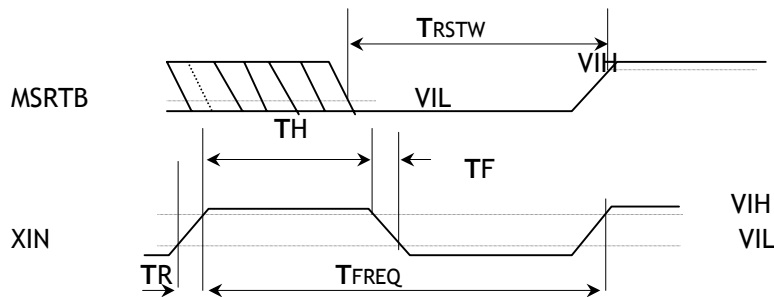
Item	Symbol	Min	Typ	Max	Unit
Input voltage "H" level	V _{IH}	0.7*VDD			V
Input voltage "L" level	V _{IL}			0.3*VDD	V
Output voltage "H" level, I _{OH} = -4mA	V _{OH}	2.4			V
Output voltage "L" level, I _{OL} = 4mA	V _{OL}			0.4	V
Earphone V _{OH} , I _{OH} = -16mA	V _{EOH}	2.4			V
Earphone V _{OL} , I _{OL} = 16mA	V _{EOL}			0.4	V
PWM V _{OH} , I _{OH} = -100mA	V _{POH}	2.4			V
PWM V _{OL} , I _{OL} = 100mA	V _{POL}			0.4	V
Input leakage current	I _L	-1		1	uA
Input capacity	C _I			10	pF

AC characteristics

MRSTB,XIN

Note : VDD = 3V±0.3 , Copacitor load = 50pF

Item	Symbol	Min	Typ	Max	Unit
MRTSB active "L" pulse width	T _{RSTW}	512			*xin
XIN frequency	1/T _{FREQ}	2		26	Mhz
XIN rising / falling time	T _R /T _F			30	ns
XIN duty	T _H /T _{FREQ}	30	50	70	%

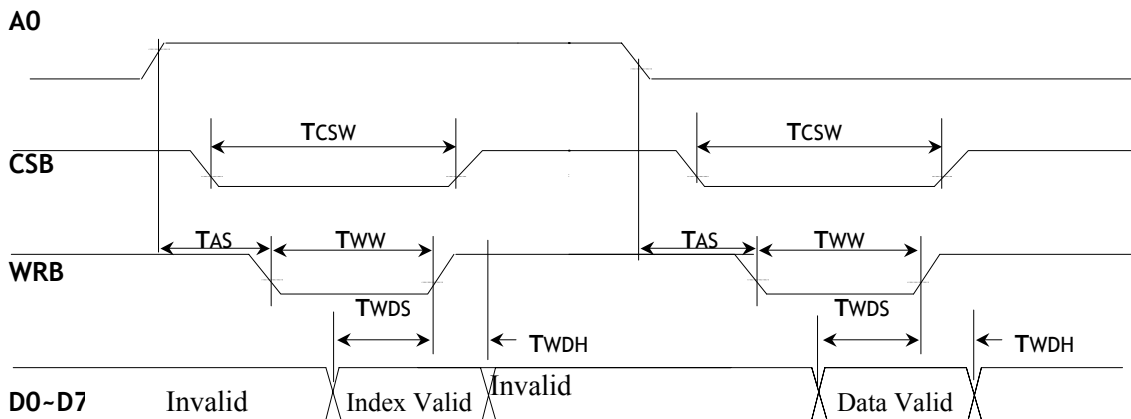




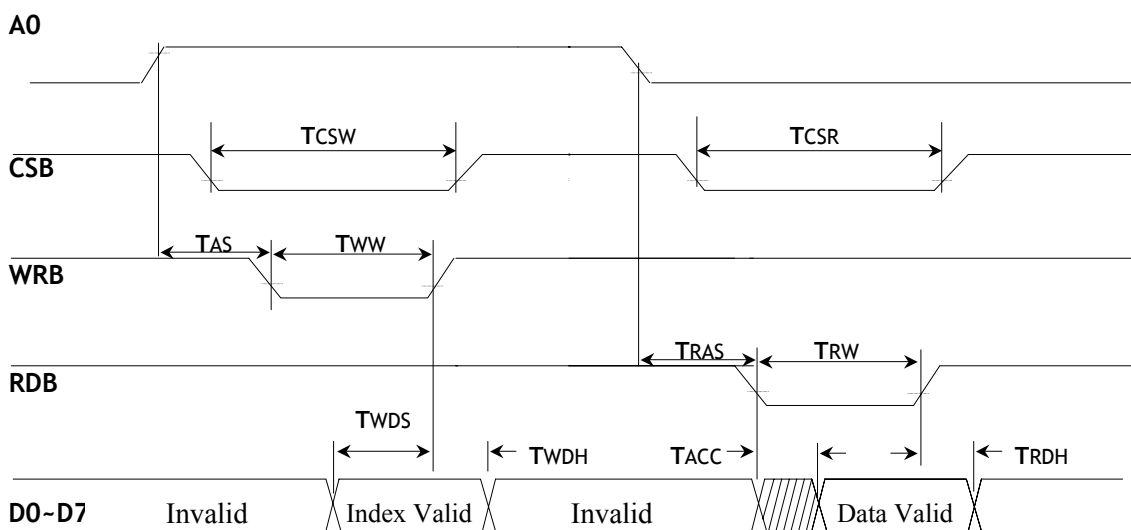
CSB, WRB, RDB, A0, IREQB, D0-D7

When XIN = 20Mhz

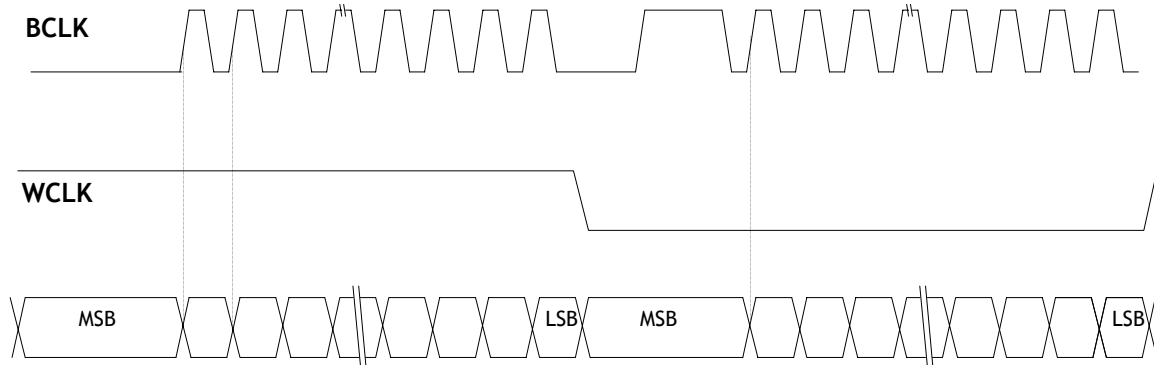
Item	Symbol	Min	Typ	Max	Unit
CSB active "L" pulse width(write)	TCSW	120			ns
Address setup time	TAS	10			ns
WRB active "L" pulse width	TWW	100			ns
Data setup time	TWDS	30			ns
Data hold time	TWDH	5			ns
CSB active "L" pulse width(read)	TCSR	120			ns
Address setup time	TRAS	10			ns
RDB active "L" pulse width	TRW	100			ns
Data read access time	TACC			70	ns
Data hold time	TRDH	10		50	ns
IREQB active "L" pulse width	TREQW	1.6			us



Timing of Write Operation



Timing of Read Operation



SDATA

BCLK,WCLK,SDATA

When XIN = 20Mhz

Item	Symbol	Min	Typ	Max	Unit
BCLK 1/Freq time	T _{BLK}		820		ns
WCLK 1/Freq time	T _{WLK}		26		us
SDATA 1/Freq time	T _{ww}	100			ns

Power consumption

Item	Min	Typ	Max	Unit
VDD section (without speaker)		20		mA
Power consumption 8Ω load and 360mW out			200	mA
Power down mode			10	uA

Note : PVDD=VDD = 3.3V

TOP =-20-85°C

Soldering temperature

Item	Min	Typ	Max	Unit
Soldering temperature	-5	235	5	°C



Chapter 8 SMF Sound Table

1) GM LITE SOUND TABLE

	PC#	CCO	Tone name
Piano	1	0	Acoustic Grand Piano
		1	Daegum
	2	0	Brigh Acoustic Piano
		1	Taepyoungso
	3	0	Electric Grand Piano
		1	Haegum
	4	0	Honkey tonk Piano
		1	Gayagum
5	0	Electric Piano 1	
	1	-	
Ch-Percussion	6	0	Electric Piano 2
	7	0	Harpichord
	8	0	Clavi
	9	0	Celesta
	10	0	Glockenspiel
	11	0	Music Box
	12	0	Vibraphone
	13	0	Marimba
Organ	14	0	Xylophone
	15	0	Tubular Bells
	16	0	Dulcimer
	17	0	Drawbar Organ
	18	0	Percussive Organ
	19	0	Rock Organ
	20	0	Church Organ
	21	0	Reed Organ
Guitar	22	0	Accordion
	23	0	Harmonica
	24	0	Tango Accordion
	25	0	Acoustic Guitar (nylon)
	26	0	Acoustic Guitar (steel)
	27	0	Electric Guitar (jazz)
	28	0	Electric Guitar (clean)
	29	0	Electric Guitar (muted)
Bass	30	0	Overdriven Guitar
	31	0	Distortion Guitar
	32	0	Guitar harmonics
	33	0	Acoustic Bass
	34	0	Electric Bass (finger)
	35	0	Electric Bass (pick)

	PC#	CCO	Tone name
Bass	36	0	Fretless Bass
	37	0	Slap Bass 1
	38	0	Slap Bass 2
	39	0	Synth Bass 1
	40	0	Synth Bass 2
String / Orchestra	41	0	Violin
	42	0	Viola
	43	0	Cello
	44	0	Contrabass
	45	0	Tremolo Stings
	46	0	Pizzicato Strings
	47	0	Orchestral Harp
	48	0	Timpani
Emsemble	49	0	String Ensemble 1
	50	0	String Ensemble 2
	51	0	SynthStrings 1
	52	0	SynthStrings 2
	53	0	Choir Aahs
	54	0	Voice Oohs
	55	0	Synth Voice
	56	0	Orchestra Hit
Brass	57	0	Trumpet
	58	0	Trombone
	59	0	Tuba
	60	0	Muted Trumpet
	61	0	French Horn
	62	0	Brass Section
	63	0	SynthBrass 1
	64	0	SynthBrass 2
Reed	65	0	Soprano Sax
	66	0	Alto Sax
	67	0	Tenor Sax
	68	0	Baritone Sax
	69	0	Oboe
	70	0	English Horn
	71	0	Bassoon
	72	0	Clarinet
Pipe	73	0	Piccolo
	74	0	Flute
	75	0	Recorder

continue next page



	PC#	CCO	Tone name
Pipe	76	0	Pan Flute
	77	0	Blown Bottle
	78	0	Shakuhachi
	79	0	Whistle
	80	0	Ocarina
Synth lead	81	0	Lead 1 (square)
	82	0	Lead 2 (sawtooth)
	83	0	Lead 3 (calliope)
	84	0	Lead 4 (chiff)
	85	0	Lead 5 (charang)
	86	0	Lead 6 (voice)
	87	0	Lead 7(fifths)
	88	0	Lead 8(bass + lead)
Synth pad	89	0	Pad 1 (new age)
	90	0	Pad 2 (warm)
	91	0	Pad 3 (polysynth)
	92	0	Pad 4 (choir)
	93	0	Pad 5 (bowed)
	94	0	Pad 6 (metallic)
	95	0	Pad 7 (halo)
	96	0	Pad 8 (sweep)
Synth SFX	97	0	FX 1 (rain)
	98	0	FX 2 (soundtrack)
	99	0	FX3 (crystal)
	100	0	FX 4 (atmosphere)
	101	0	FX 5 (brightness)
	102	0	FX 6 (goblins)
	103	0	FX7 (echoes)
	104	0	FX 8 (sci-fi)
Ethnic	105	0	Sitar
	106	0	Banjo
	107	0	Shamisen
	108	0	Koto
	109	0	Kalimba
	110	0	Bag pipe
	111	0	Fiddle
	112	0	Shanai
Percussive	113	0	Tinkle Bell
	114	0	Agogo
	115	0	Steel Drums

	PC#	CCO	Tone name
Percussive	116	0	Woodblock
	117	0	Taiko Drum
	118	0	Melodic Tom
	119	0	Synth Drum
	120	0	Reverse Cymbol
SFX	121	0	Guitar Fret Noise
	122	0	Breath Noise
	123	0	Seashore
	124	0	Bird Tweet
	125	0	Telephone Ring
	126	0	Helicopter
	127	0	Applause
	128	0	Gunshot

PC# :
CCO :



2) Percussion Map(Channel 10 PC#1)

Note	PC#1:STANDARD Set		
27	-	67	High Agogo
28	-	68	Low Agogo
29	-	69	Cabasa
30	-	70	Maracas
31	-	71	Short Hi Whistle [EXC2]
32	-	72	Long Low Whistle [EXC2]
33	-	73	Short Guiro [EXC3]
34	-	74	Long Guiro [EXC3]
35	Kick Drum 2/Jazz BD2	75	Claves
36	Kick Drum 1/Jazz BD1	76	High Wood Block
37	Side Stick	77	Low Wood Block
38	Snare Drum 1	78	Mute Cuica [EXC4]
39	Hand Clap	79	Open Cuica [EXC4]
40	Snare Drum 2	80	Mute Triangle [EXC5]
41	Low Tom 2	81	Open Triangle [EXC5]
42	Closed Hi-hat [EXC1]	82	-
43	Low Tom 1	83	-
44	Pedai Hi-hat [EXC1]	84	-
45	Mid Tom 2	85	-
46	Open Hi-hat [EXC1]	86	-
47	Mid Tom 1	87	-
48	High Tom 2	88	-
49	Cymbal 1	89	-
50	High Tom 1		
51	Ride Cymbal 1		
52	Chinese Cymbal		
53	Ride Bell		
54	Tambourine		
55	Splash Cymbal		
56	Cowbell		
57	Crash Cymbal 2		
58	Vibra - slap		
59	Ride Cymbal 2		
60	High Bongo		
61	Low Bongo		
62	Mute High Conga		
63	Open High Conga		
64	Low Conga		
65	High Timbale		
66	Low Conga		



Percussion Map(Channel 10 PC#2)

Note	PC#2:HWASS Set	
27	Muted Ggangary	67 High Agogo
28	Ggangary	68 Low Agogo
29	Jing	69 Cabasa
30	Muted Jing	70 Maracas
31	Jangu	71 Short Hi Whistle [EXC2]
32	Muted Jangu	72 Long Low Whistle [EXC2]
33	BUK	73 Short Guiro [EXC3]
34	Muted Jangu	74 Long Guiro [EXC3]
35	Kick Drum 2/Jazz BD2	75 Claves
36	Kick Drum 1/Jazz BD1	76 High Wood Block
37	Side Stick	77 Low Wood Block
38	Snare Drum 1	78 Mute Cuica [EXC4]
39	Hand Clap	79 Open Cuica [EXC4]
40	Snare Drum 2	80 Mute Triangle [EXC5]
41	Low Tom 2	81 Open Triangle [EXC5]
42	Closed Hi-hat [EXC1]	82 d Ggangary
43	Low Tom 1	83 ggangary
44	Pedai Hi-hat [EXC1]	84 Jing
45	Mid Tom 2	85 uted Jing
46	Open Hi-hat [EXC1]	86 Jangu
47	Mid Tom 1	87 ted Jangu
48	High Tom 2	88 BUK
49	Cymbal 1	89 ted Jangu
50	High Tom 1	
51	Ride Cymbal 1	
52	Chinese Cymbal	
53	Ride Bell	
54	Tambourine	
55	Splash Cymbal	
56	Cowbell	
57	Crash Cymbal 2	
58	Vibra - slap	
59	Ride Cymbal 2	
60	High Bongo	
61	Low Bongo	
62	Mute High Conga	
63	Open High Conga	
64	Low Conga	
65	High Timbale	
66	Low Conga	



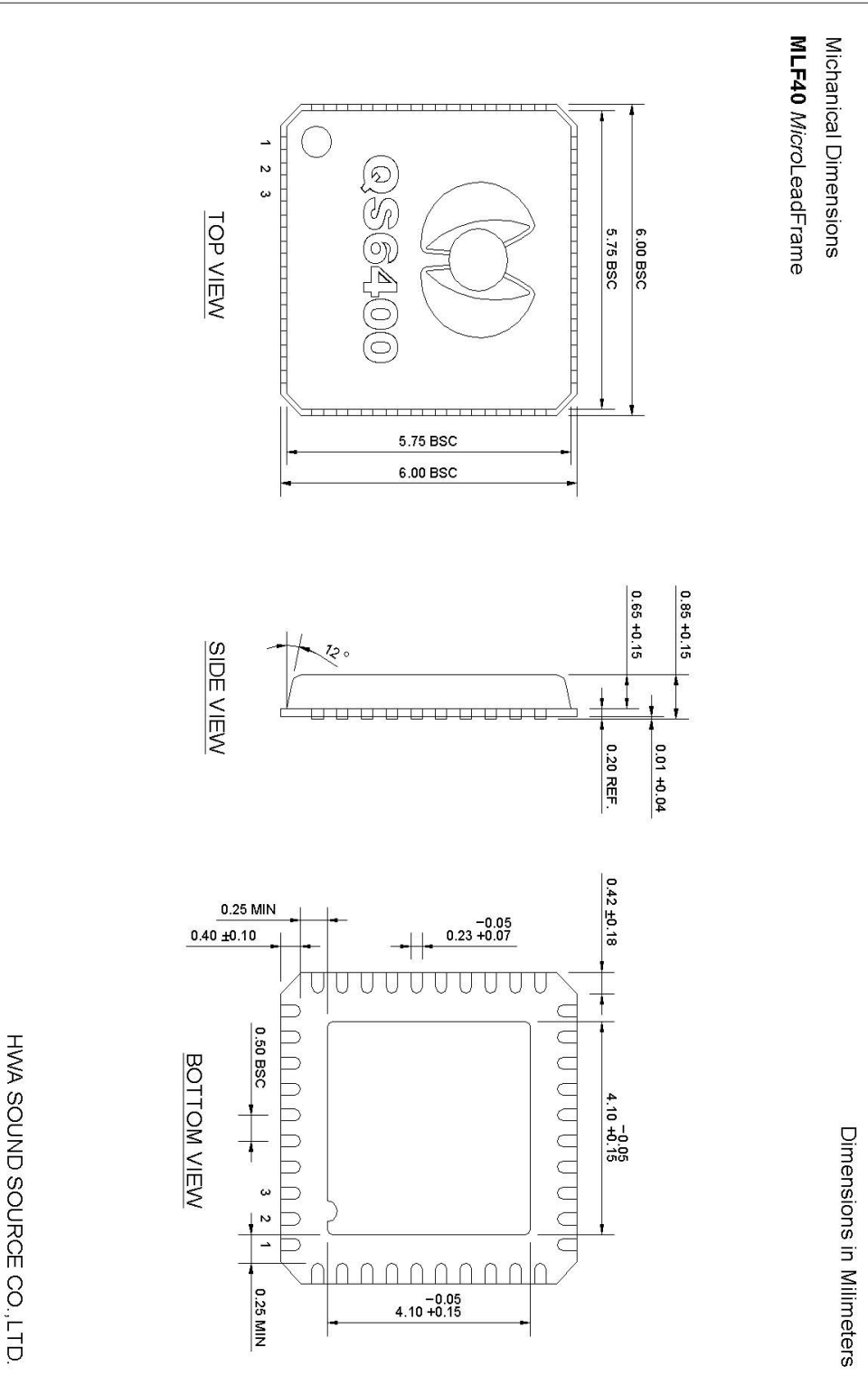
MIDI Implementation Chart

Function		Transmitted	Recognized	Remarks
Basic	default	X	1-16	
Channel	Changed	X	1-16 Each	
Mode	Default	X	Mode 1*	
Note number		X	21 ~108	
Velocity	ON	X	0	
Velocity	OFF	X	0	
After Touch	Key's	X	X	
After Touch	Chn's	X	X	
Pitch Bender		X	0	
Control Change	0,32	X	0	Bank Selection
	1	X	0	Modulation
	6,38	X	0	Data entry(100,101 Only)
	7	X	0	Volume
	10	X	0	Panpot
	11	X	0	Expression
	64	X	0	Sustain
	66	X	X	Soft
	67	X	X	Sustanuto
	100,101	X	0	RPN LSB MSB(00,00 Only)
	120	X	0	All sound off
	121	X	0	Reset all controller
123	X	0	All note off	
Program	Change	X	0-127	
System	Exclusive	X	X	
Common	Song position	X	X	
	Song selection	X	X	
	Tune	X	X	

Mode 1* : Omni ON / Poly ON



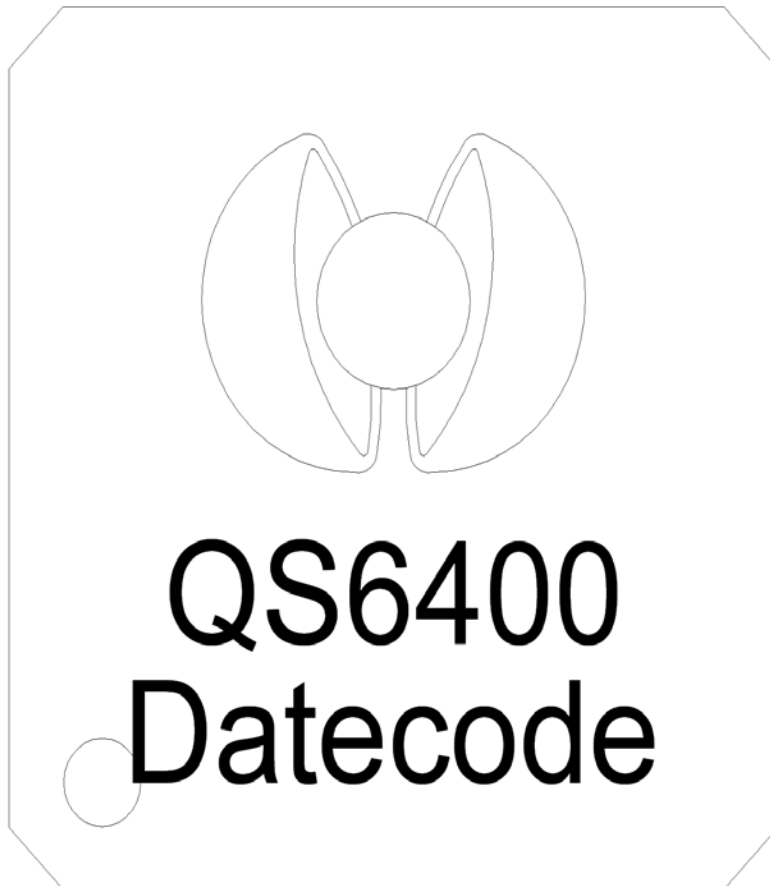
Chapter 9 Outline Dimensions





Chapter 10 Marking

- Part_number = QS6400
 - Datecode = Year/Numbers of week
- ex) Production day = 2003/1/07
QS6400
"0302"



History of Revision.

Date	Change of Contents	Revision Number
03-03-31	-	Ver 1.0
03-09-01	Revision the "Chapter 5-1 Register Table"	-
04-03-30	Added the "Chapter 5-1 Register Table and Detail"	Ver 2.0