

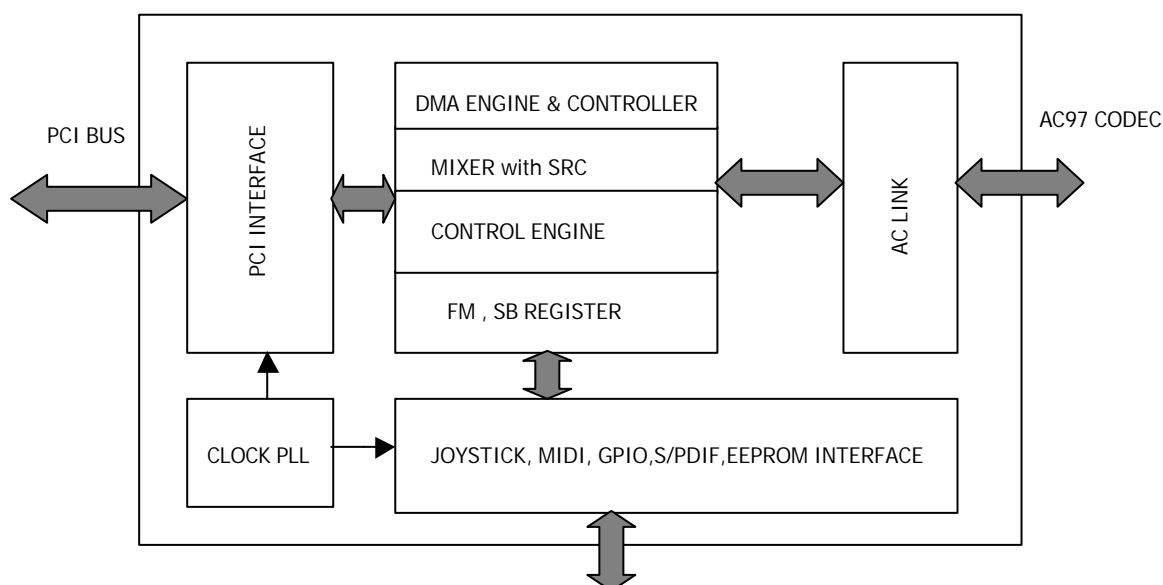
## FEATURES

- . Full legacy audio compatibility in DOS and Windows games using QDSP legacy support through DDMA, PC/PCI, Serial IRQ
- . Hardware SRC( sample rate converter) with more than 20,000 volume level control for each digital input source
- . 20 voice FM Synthesizer, high resolution Game Port, MIDI, GPIO, EEPROM S/PDIP IN and OUT Port support
- . Hardware Volume control support
- . Full duplex operation support
- . PCI 2.1 BUS Master/Slave along with scatter and gather capability
- . Windows 95,98, Windows NT 4.0 and 5.0 (WDM) driver support with PC '98 and PC '99 Compliance and Software Wave Table Support

# QDSP PCI AUDIO

- . AC-link supports Multi Channel Audio output support with 18 bit resolution

The HWA3000 is a PCI Audio controller using high performance QDSP Technology. The HWA3000 supports Legacy games and is a high quality audio solution for add-on and motherboard designs combined with QDSP software wave table and audio stations. The legacy audio compatibility is supported by DDMA, PC/PCI, and Serial IRQ solutions. Also, the HWA3000 controller supports multi-channel output support for different applications along with 20,000 level volume control and high quality 18 bit output data. The product includes the PCI Plug and Play function, FM synthesizer, and soft and hard ware wave table support capability to deliver true midi music. The HWA3000 is compliant with Microsoft's PC98, PC99 audio requirements and Legacy audio support. The HWA3000 has two different package types to support dynamic customer requirements.



## Overview

The HWA3000 is a single, highly integrated, low cost PCI audio controller with Legacy game compatibility.

The HWA3000 is partitioned into 4 functional blocks: PCI Interface, FM Synthesis, Audio system engine and peripheral interface.

The PCI Interface provides a physical connection to the bus. Internally, the PCI interface has several smaller blocks to meet PCI specifications, such as PCI PnP, device configuration, DMA setting, interrupt handling, and Master/Target read/write operations. The PCI interface also contains base address registers, provided to set up the internal operation register and to execute chip operation.

The FM Synthesis provides a full range of compatibility for industrial standard FM based DOS games and other software.

The HWA3000's Legacy support and Windows Sound System support is further enhanced by the audio system engine to perform several key operations of DMA function and data transfer. The internal DMA block provides various dedicated hardware that perform data transfer, to and from the system memory, support simultaneous playback, record, and support modem interfacing. It also supports software wave table without having to use the OS to convert data. The dedicated wave table interface using DMA or a peripheral interface provides performance enhancements and advantages to deliver MIDI sound during other sound reproductions.

The Legacy support provides an internal SB interface block to make DOS mode and Windows games compatible. The QDSP DDMA, PC/PCI, and serial IRQ interface provide Legacy I/O addresses and IRQ access to allow Legacy support in motherboard and add-in card designs.

The Audio system block also provides a full range of sample rate converters and digital mixers to deliver high quality sound beyond today's specification. It supports various types of data formats and multi-channel hardware volume controls. The digital mixer provides dedicated hardware, which uses QDSP sound products to perform superb sound reproduction and deliver real world sound generation without compromising the quality of the audio. It also provides a variety of output data structures to meet the next generation of AC97 codec specifications and capabilities.

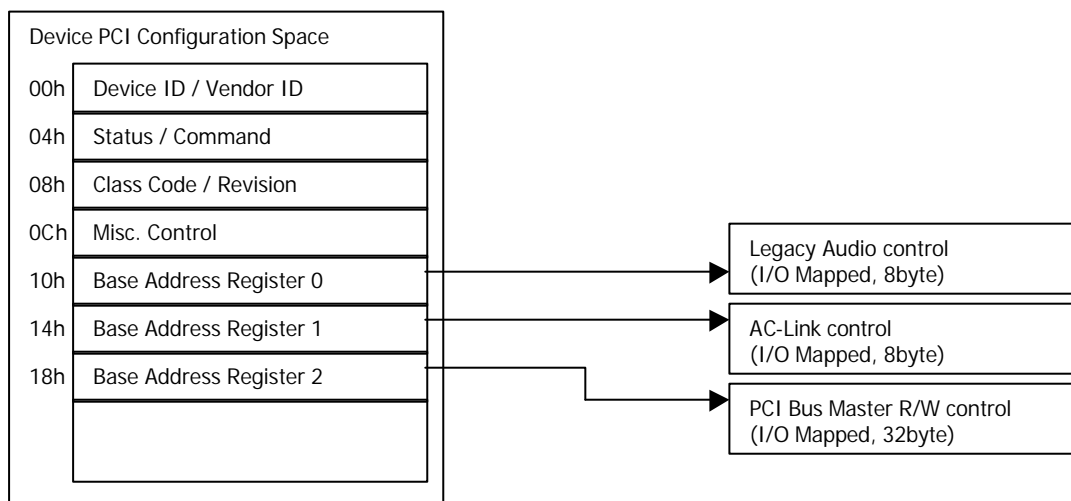
The peripheral interface provides an even further enhancement of the system using a hardware volume control interface, S/PDIF in and out interface, 128 level MIDI UART interface, high quality GAME port, General Purpose I/O port, EEPROM interface for variable system, subsystem support, and Multi-channel AC link.

## Host Interface

The HWA3000 host interface consists of three individual interface blocks that are I/O mapped into host address space. These interface blocks are located within the host 32-bit physical address space. The locations of the interface blocks are defined by the addresses programmed into the three base Address Registers in the PCI Configuration Space. The system's Plug and Play BIOS sets up these base addresses. The Base Address 0 holds the

Legacy audio configuration, control and status registers for the device. The Base Address 1 maps the AC97 link control register. The Base Address 2 maps the PCI Master control register. The PCI bus interface complies with the PCI Local Bus Specification. Below is a diagram which depicts the relationship between the Base Address Registers of the HWA3000 PCI Configuration Space and the host I/O map.

## Host Interface Base Address Registers



## PCI bus interface

The HWA3000 is a single function PCI device.

### Vendor ID

There are two methods of loading the Subsystem ID and Subsystem Vendor ID. During power-up, When the external EEPROM mode is selected, the HWA3000 loads data from the external EEPROM. To minimize costs, the HWA3000 can load the Subsystem ID and Subsystem Vendor ID from internal ROM without using an external EEPROM.

**PCI Configuration Register  
Summary Table***Table 1: PCI Configuration Register Summary*

Host Config Address	Host R/W	Power-on Value	Description
0x01~00	R	0x14AA	Vendor ID
0x03~02	R	0x3000	Device ID
0x05~04	R/W	0x0000	PCI Command Register
0x07~06	R/W	0x0280	PCI Status Register
0x08	R	0x00	Revision ID Register
0x0B~09	R	0x040100	Class Code (multimedia audio device)
0x0C	R	0x00	Cache Line Size Register (not implemented)
0x0D	R/W	0x00	Latency Timer
0x0E	R	0x00	Header Type
0x0F	R	0x00	BIST (not implemented)
0x13~10	R/W	0x00000001	I/O Base Register 0
0x17~14	R/W	0x00000001	I/O Base Register 1
0x1B~18	R/W	0x00000001	I/O Base Register 2
0x2D~2C	R	0x14AA	Subsystem Vendor ID (Changeable by EEPROM)
0x2F~2E	R	0x3000	Subsystem ID (Changeable by EEPROM)
0x34	R	0x00	Capabilities Pointer
0x3C	R/W	0x00	Interrupt Line Register <sup>1</sup>
0x3D	R	0x01	Interrupt Pin Register (INTA#)
0x3E	R	0x05	Min Grant PCI Burst period
0x3F	R	0x19	Max Latency PCI grand period
0x41~40	R/W	0x907F	Legacy Audio Control

Table 1. PCI configuration register

### Legacy Audio Address Map

This section describes all the Legacy audio control registers supported by the HWA3000.

- SB base: 0x220, 0x240
- OPL-3 base: 0x388
- Game base: 0x201
- MPU base: 0x300, 0x310, 0x320, 0x330

### OPL-3

Host Offset	R/W	Width	Description
SB base + 0	R	8	Status read
SB base + 0	W	8	Address bank0 write
SB base + 2	W	8	Address bank1 write
SB base + 1 SB base + 3	W	8	Data write
SB base + 8	R	8	Status read
SB base + 8	W	8	Address bank0 write
SB base + 9	W	8	Data write
OPL base + 0	R	8	Status read
OPL base + 2	W	8	Address bank1 write
OPL base + 1 OPL base + 3	W	8	Data write

### SB Pro I/O

Host Offset	R/W	Width	Description
SB base + 6	W	8	SB DSP reset
SB base + A	R	8	SB DSP read data port
SB base + C	W	8	SB DSP write data port
SB base + C	R	8	SB DSP write buffer status
SB base + E	R	8	SB DSP read buffer status

**SB Pro Mixer**

Host Offset	R/W	Width	Description
SB base + 4	W	8	SB mixer address port
SB base + 5	R/W	8	SB mixer data port

**Game Port**

Host Offset	R/W	Width	Description
Game base + 0	R/W	8	Conventional game port

**MPU-401**

Host Offset	R/W	Width	Description
MPU base + 0	R/W	8	Data port
MPU base + 1	R	8	Status port
MPU base + 1	W	8	Command port

Table 2. Legacy Audio register map

### EEPROM Interface

The EEPROM configuration interface permits a connection of an optional external EEPROM device to provide power-up configuration information. Proper functionality is not dependent on the external EEPROM. Although, in some applications, power-up configuration settings other than the default values can be required to support specific Operating System compatibility requirements.

Following a hardware reset, when the E2PSELECT pin is low, an internal state machine in the HWA3000 will detect the presence of an external EEPROM device. The data from the EEPROM is loaded into the Subsystem ID and Subsystem Vendor ID fields in the Configuration Space. The Vendor ID and Device ID are loaded in the Configuration Space as well. Software to read/write the EEPROM is provided by HWA Sound Source co., Ltd.

In the case where an application does not need an external EEPROM, the EEPROM interface pin can use a general purpose in/out pin.

The HWA3000 external EEPROM Interface.

Support device : 93C46

Format : 8BIT BYTE

( ORG pin of EEPROM tied to GND)

### General Purpose I/O Pins

To serve various functions dependent on the HWA3000 driver, seven pins are internally multiplexed. These pins are listed below:

GPIO\_0/E2PCS : EEPROM Chip select  
GPIO\_1/E2PSK : EEPROM serial clock  
GPIO\_2/E2PDI : EEPROM Data In  
GPIO\_3/E2PDO : EEPROM Data Out  
GPIO\_4/VOLUP : H/W volume up  
GPIO\_5/VOLDOWN : H/W volume down  
GPIO\_6/VOLMUTE : H/W volume mute

### OPL3 FM synthesis

The HWA3000 includes FM synthesis hardware. This is useful for real DOS mode applications, due to the unavailability of software wavetable synthesis in this mode. FM is functionally compatible with the YAMAHA YMF262.

### MPU-401 interface

This interface is compatible with the MPU-401 standard. It takes serial MIDI input on the RXD pin, converts it to 8-bit parallel data, and stores it in a 128 stage FIFO for retrieval by the host system. It also transmits parallel data from the host system to the TXD pin. The baud rate is 31250 bits per second.

### Game port (Joystick) Interface

The game port supports industry standards with a 16 level speed selection function. Four "coordinate" channels and four "button" channels are supported by the game port. The "coordinate" channels provide game port positional information, and the "button" channels provide user button event information to the host.

### Hardware Volume Control

The hardware volume control supports volume up, volume down and volume mute. VOL UP is for increasing volume, VOL DOWN is for decreasing volume, and VOL MUTE is for muting volume. In real DOS mode, the hardware volume control block can directly write volume data through the AC-link without the service interrupt routine.

Each of these pins are shared as general purpose Input/Output.

## Zoomed Video Port (f S)

The Zoomed Video port is a standard bus for the PC-Card (PCMCIA) that directly outputs a digital signal to be connected to a video or audio chip on the PC system. The ZV port format is generally referred to as I2C format. The Master clock is  $384 \times F_s$  or  $256 \times F_s$ . The HWA3000 does not use the ZV port master clock but rather reads the sample rate from a register set by the driver. The sample rate converter of the HWA3000 can accept data from the ZV port in the following sampling rates: 32K, 44.1K and 48K. The ZV Port data is sent through a sample rate converter and resampled at 48kHz before it is digitally mixed with the main audio signal. This mechanism is possible through a separate digital volume control.

The HWA3000 also supports digital interfacing with the QS1000 hardware wavetable synthesis chip, by changing a register bit. Its timing diagram differs from that of the ZV port.

The signal diagram and pin names are shown below.

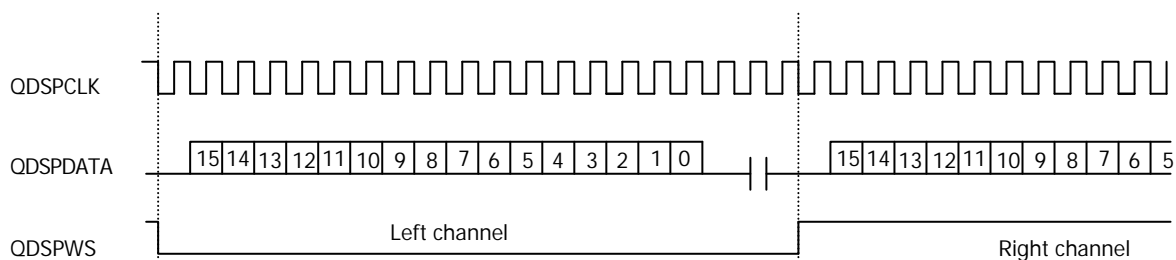


Fig. 1 Zoomed Video port timing

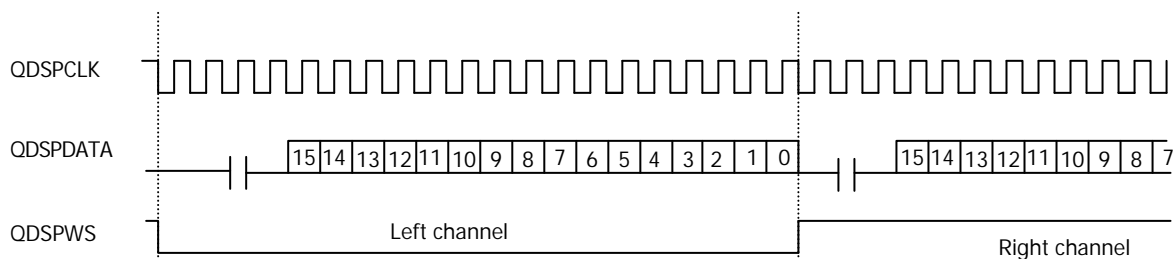


Fig. 2 Interface of the QS1000 hardware wavetable synthesis chip

### AC-link interface

The HWA3000 provides the AC-link interface with an AC' 97 CODEC and can also connect multiple CODECs for multi-channel processing. When applications need a 4-channel voice play function, the HWA3000 can create two kinds of connections. One solution is to use multi-channel CODECs like Sigmatel STMA9708. It has a 4 channel DAC. The other solution is using two CODECs with 2 channel DACs. It is compatible with multi-channel CODEC interfaces. The multi CODEC interface can control each CODEC volume separately. The HWA3000 AC-link can carry voice play data up to 6 channels. This means the HWA3000 can control difference voices and difference volumes for up to 6 speakers. The HWA3000 AC-link is comprised of 7 pins, which are described below.

F24MOUT : 24MHz clock output.  
RSTOUTN : AC-Link reset output  
SYNCPAD : Sync output  
BITCLK : Bit clock input  
SDOUT : Serial data output  
SDINA : Primary CODEC data input  
SDINB : Secondary CODEC data input

### DMA emulation

#### Distributed DMA interface

HWA3000 provides the following registers to support DDMA.

The HWA3000 supports 8-bit DMA transfers only.

Address	R/W	Description
Base + 00h	W	Base Address 0 - 7
Base + 00h	R	Current Address 0 - 7
Base + 01h	W	Base Address 8 - 15
Base + 01h	R	Current Address 8 - 15
Base + 02h	W	Base Address 16 - 23
Base + 02h	R	Current Address 16 - 23
Base + 03h	W	Base Address 24 - 31
Base + 03h	R	Current Address 24 - 31
Base + 04h	W	Base Word counter 0 - 7
Base + 04h	R	Current Word counter 0 - 7
Base + 05h	W	Base Word counter 8 - 15
Base + 05h	R	Current Word counter 8 - 15
Base + 06h	W	Base Word counter 16 - 23
Base + 06h	R	Current Word counter 16 - 23
Base + 07h	N/A	Reserved
Base + 08h	W	Command
Base + 08h	R	Status
Base + 09h	W	Request
Base + 0ah	N/A	Reserved
Base + 0bh	W	Mode
Base + 0ch	N/A	Reserved
Base + 0dh	W	Master clear
Base + 0eh	N/A	Reserved
Base + 0fh	R/W	Multi-channel mask

Table 3. DDMA register

### PC/PCI interface

The HWA3000 provides two signals, PREQ# and PGNT#, to detect the PC/PCI. The HWA3000 declares PCPCI# to being "high" using the PCICLK corresponding to the DMA channel it is going to use. Only 8-bit DMA channels are supported by the HWA3000. See Fig. 3 for the timing diagram.

b2,b1,b0	PGNT# coding
0 0 0	DMA channel 0
0 0 1	DMA channel 1
0 1 0	DMA channel 2
0 1 1	DMA channel 3
1 0 0	reserved
1 0 1	DMA channel 5
1 1 0	DMA channel 6
1 1 1	DMA channel 7

Table 4. PC/PCI DMA channel number

### Serialized IRQ (SIRQ)

In order to support PCI Plug and Play, the HWA3000 provides a serialized IRQ. The serialized IRQ is not a PCI standard pin. Designers route SIRQ to HWA3000 pin 85 directly.

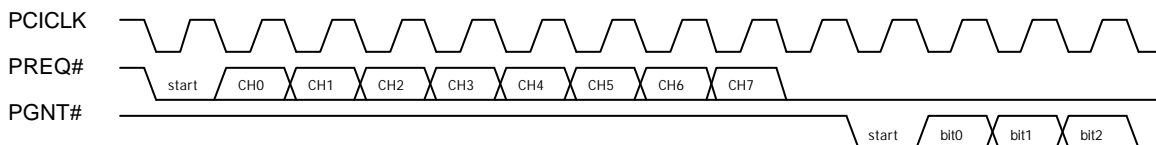
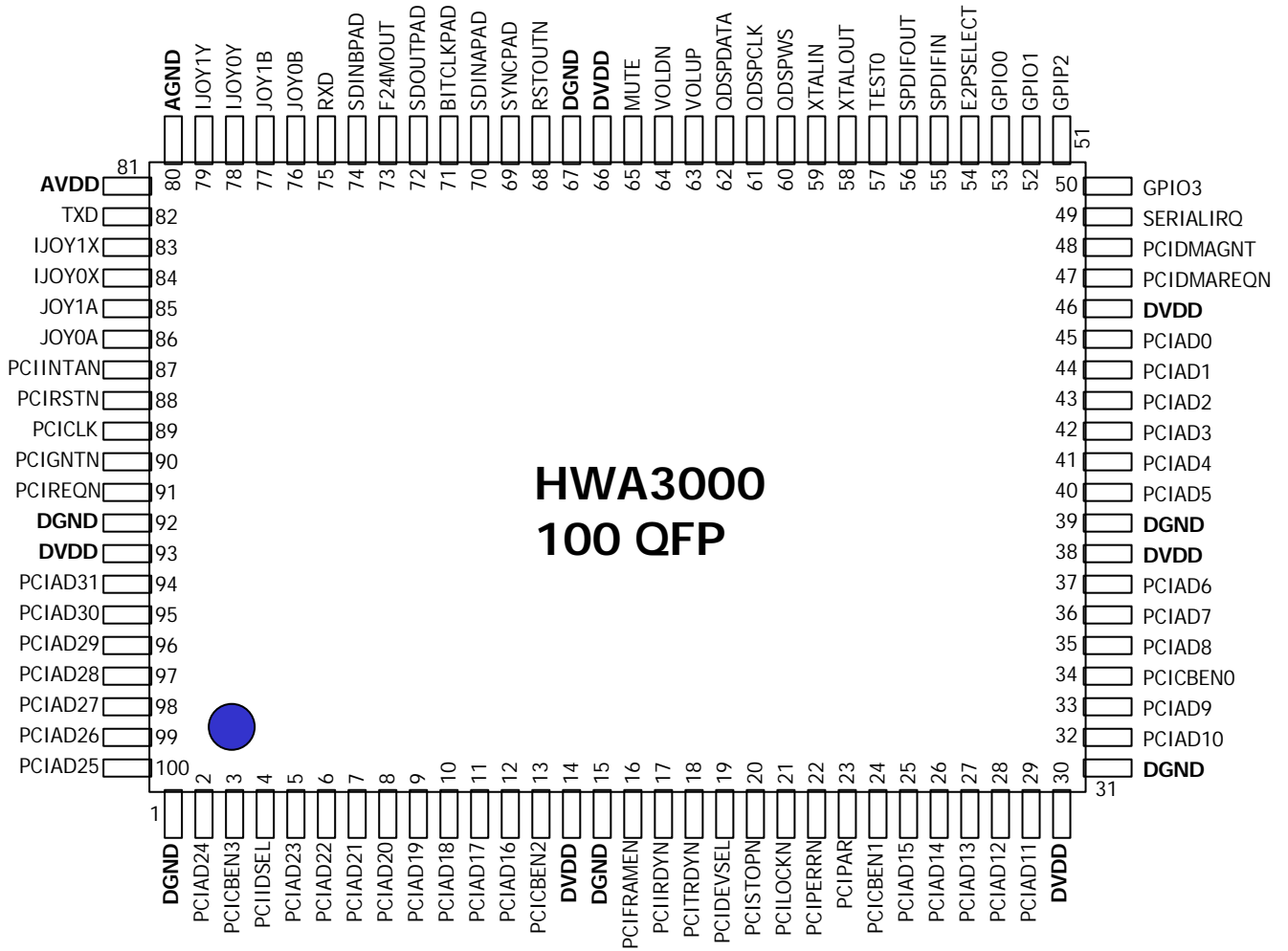


Fig. 3 PC/PCI DMA Timing

## PIN configuration (100 QFP)



## PIN description

### PCI Bus Interface

**PCICLK : PCI Bus Clock, In**

This is the PCI bus clock for timing all PCI transactions. All PCI synchronous signals are generated and sampled relative to the rising edge of this clock.

**PCIRSTN : PCI Device Reset, In**

This is the PCI bus master reset.

**PCIGNTN : Master Grant, Tri I/O**

This is driven by the system arbiter to indicate that HWA3000 has control of the PCI bus.

**PCIIDSEL : Initialize Device Select, In**

This is used as a chip select during PCI Configuration Space read and write cycles.

**PCIAD[31:0] : Address/Data Bus, Tri-State I/O**

Forms the multiplexed address/data bus for PCI interface.

**PCICBEN[3:0] : Command/Byte Enable Bus, Tri-State I/O**

Four pins constitute the multiplexed command / byte enable for the PCI interface. The cycle type is indicated by these pins during the address phase of a transaction. For the data phases of a transaction, active low byte enable information for the current data phase is indicated. During bus mastering operation, these pins are outputs, and during slave operation they are inputs.

**PCIPAR : Parity, Tri-State I/O**

Indicates even parity across PCIAD[31:0] and PCICBEN[3:0] for both addresses and data phases. The signal is delayed one PCI clock from either the address or data phase for which parity is generated.

### External Mix Control (GPIO)

**VOLUP (GPIO\_4) : Volume Up Button, Tri-I/O (Schmitt), Double Bonding**

This is the volume up button control input. May also serve as a general purpose input if its primary function is unnecessary. If VOLDN is disconnected, it will be pulled to its inactive state due to the internal 20K $\Omega$  pull-up resistor.

**PCIFRAMEN : Cycle Frame, Sustained Tri-I/O**

This is driven by the current PCI bus master. Indicates the beginning and duration of a transaction.

**PCIIRDYN : Initiator Ready, Sustained Tri-I/O**

This is driven by the current PCI bus master. Indicates that the initiator is ready to transmit or receive data (complete the current data phase).

**PCITRDYN : Target Ready, Sustained Tri-I/O**

This is driven by the current PCI bus master. Indicates that the initiator is ready to transmit or receive data (complete the current data phase).

**PCISTOPN : Target Ready, Sustained Tri-I/O**

This is driven by the current PCI bus master. Indicates a request to the master to stop the current transaction.

**PCIDEVSELN : Device Select, Sustained Tri-I/O**

This is driven by the PCI bus target device. Indicates that it has decoded the address of the current transaction as its own chip select range.

**PCIPERRN : Parity Error, Sustained Tri-I/O**

This is used for reporting data parity errors on the PCI bus.

**PCIREQN : Master Request, Tri-State I/O**

This indicates to the system arbiter that the HWA3000 is requesting access to the PCI bus. This pin in high-impedance when PCIRSTN is active.

**PCIINTAN : Host Int. A, Open Drain Output**

This is the level triggered interrupt pin. Dedicated to servicing internal device interrupt sources.

**VOLDN (GPIO\_5) : Volume Down Button, Tri-I/O (Schmitt), Double Bonding**

This is the volume down button control input. May also serve as a general purpose input if its primary function is unnecessary. If VOLDN is disconnected, it will be pulled to its inactive state due to the internal 20K $\Omega$  pull-up resistor.

### AC '97 Interface

**SYNCPAD : AC-Link Frame Sync, Output**

This is the framing clock for serial audio data. It is an output that indicates the 48KHz framing for the AC-Link. Induces a warm reset of the AC-Link when down.

High : Slot 0

Low : Slot 1-12

**BITCLKPAD : AC-Link Bit Clock, Input**

This is the master timing clock for serial audio data. It is an input that drives the timing for the AC-Link interface. Provides the source clock for HWA3000.

**SDOUTPAD : AC-Link Data Out, Output**

This is the serial data output for HWA3000. It Provides a register interface and playback audio data Path to both Primary/Secondary Codecs.

**SDINAPAD : Primary Codec Data In, Input**

Serial data input from the Primary Codec to the HWA3000 for the purpose of register reads and capture of audio data streams.

**PCISTOPN : Target Ready, Sustained Tri-I/O**

This is driven by the current PCI bus master to indicate a request to the master to stop the current transaction.

**SDINBPAD : Secondary Codec Data In, Input**

Serial data input from the Secondary Codec to the HWA3000 or general purpose input. Target is selected through the SPMC register. As a general purpose I/O pin, it also supports extended capability. If the pin is not in use, an external resistor of  $\geq 50K\Omega$  attached to the ground.

**RSTOUTN : AC-Link Reset, Output**

This is the AC-Link and Codec reset pin. The pin acts as the logical OR of the PCI reset pin PCIRSTN. When low, it forces all Codecs attached to the AC-Link into a cold reset mode.

### Game Port

**IJOY0X, IJOY0Y, IJOY1X, IJOY1Y :****Joystick A and B X/Y Coordinates, I/O**

4 axis coordinates for the joystick port.

**JOY0A, JOY0B, JOY1A, JOY1B :****Joystick A and B Button Inputs, Input**

4 button switches for the joystick port.

### GPIO / E<sup>2</sup>PROM Interface

**GPIO\_2 (E2PDI) : EEPROM Data Line / PC/PCI Grant, I/O**

This is the data line for external serial EEPROM containing device configuration data for expansion card designs. In the presence of an external EEPROM, a  $4.7K\Omega$  pull-up resistor is required. This is the PC/PCI serialized grant input in motherboard designs using PC/PCI. Otherwise, this pin may be used as a general purpose input or open drain output.

**GPIO\_3 (E2DO) :****General Purpose Input/Output 3, I/O**

This is a general purpose I/O pin that is powered by the PCI power supply. Backward compatibility is possible as the pin powers up in a high impedance state. The remaining general purpose I/O must be tied high through its own  $10K\Omega$  resistor.

## CHARACTERISTICS and SPECIFICATION

### Absolute Maximum ratings

PARAMETER	SYMBOL	MIN		MAX	UNIT
	<b>PCI_VDD</b>			4.2	V
	<b>A_VDD</b>			4.2	V
<b>DIGITAL INPUT VOLTAGE</b> (note 1)				Vdd+0.3	V
<b>TOTAL POWER DISSIPATION</b> (note 2)				1.0	W
<b>INPUT DC CURRENT PER PIN</b> (note 3)				10	mA
<b>OUTPUT DC CURRENT PER PIN</b>				50	mA
<b>OPERATING AMBIENT TEMPERATURE</b> (note 4)		-50		125	C
<b>STORAGE TEMPERATURE</b>		-60		140	C

( PCI\_GND=A\_GND= 0 V ) , all voltage ratings are respect to 0 V.

- NOTE 1. The power supply is applied using recommend maximum value.  
 2. The power generated by AC/DC output loading  
 3. All the input pins except power supply pins.  
 4. At ambient temperature, must be limited power. See recommended operating condition.

### RECOMMENED OPERATING CONDITION

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
<b>POWER SUPPLIES</b>	<b>PCI_VDD</b>	3.0	3.3	3.6	V
	<b>A_VDD</b>	3.0	3.3	3.6	V
<b>OPERATING AMBIENT TEMPERATURE</b>	<b>Ta</b>	0	25	70	V

**WARNING:** Operation beyond these conditions may result in permanent damage to device.

( PCI\_GND=A\_GND= 0 V ) , all voltage ratings are respect to 0 V

### Electrical Characteristics

#### Absolute Maximum Rating

Item	Symbol	Rating	Unit
Power Supply Voltage	VDD	-0.3 --- 7.0	V
Input Voltage	Vin	-0.3 --- VDD+0.3	V
Operating Ambient Temperature	Top	0 -- 70	C
Storage Temperature	Tstg	-50 -- 125	C

#### Recommended Operating Condition

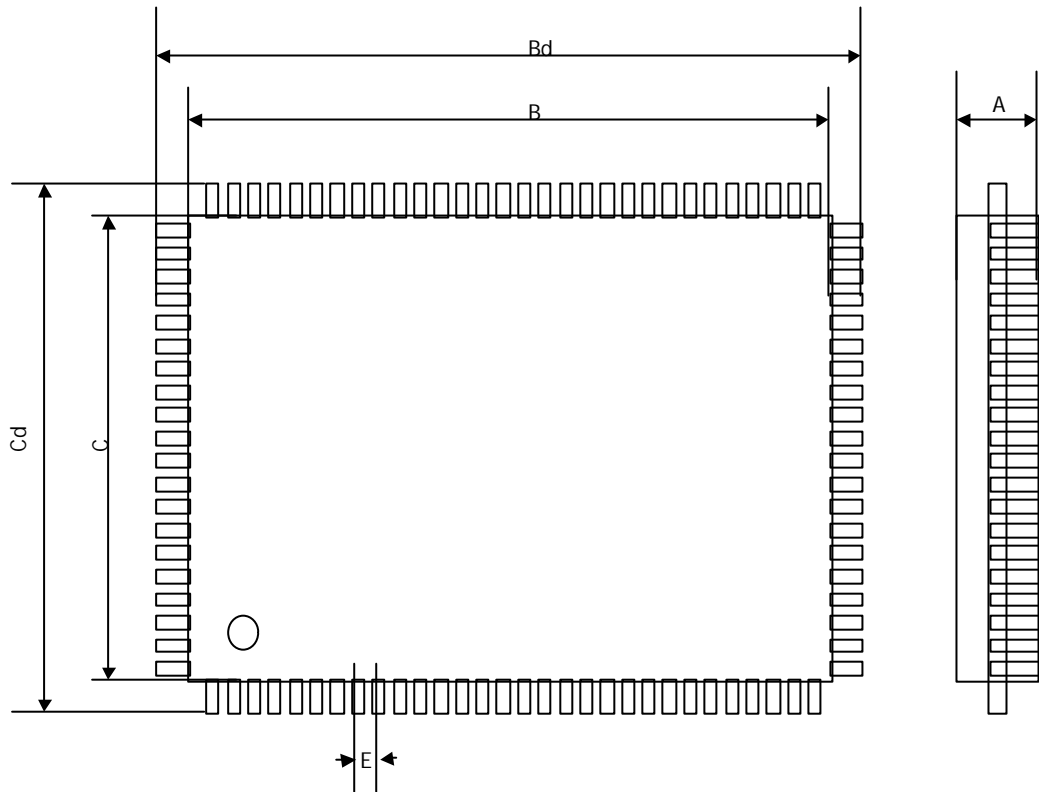
Item	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	VDD	4.75	5.0	5.25	V
Operating Ambient Temperature	Top	0	25	70	C

#### DC Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High Level Input Voltage (CMOS) except Joy0X,0Y,1X,1Y	Vih		2.5			V
Low Level Input Voltage(CMOS) except Joy0X,0Y,1X,1Y	Vil				1.5	V
High Level Input Voltage (Joy0X,0Y,1X,1Y)	Vih					V
Low Level Input Voltage (Joy0X,0Y,1X,1Y)	Vil					V
High Level Input Voltage (TTL)	Vih		2.0			V
Low Level Input Voltage(TTL)	Vil				0.4	V
Input High Leakage Current	Iih				10	uA
Input Low Leakage Current	Iil				-10	uA
High Level Output Voltage(CMOS)	Voh	Ioh = -4mA	4.0			V
Low Level Output Voltage(CMOS)	Vol	Iol= 4mA			0.4	V
High Level Output Voltage(TTL)	Voh	Ioh = -4mA	4.0			V
Low Level Output Voltage(TTL)	Vol	Iol= 4mA			0.4	V
Input Pin Capacitance	Cin		5		15	pF
Clock Pin Capacitance	Cclk		5		15	pF
IDSEL Pin Capacitance	Cidsel		5		15	pF

## Mechanical Packages

### 100 PQFP, Plastic Quad Flat Package



Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	2.57	2.72	2.87	0.101	0.107	0.113
B	19.90	20.00	20.10	0.783	0.787	0.791
Bd	23.00	23.20	23.40	0.905	0.913	0.921
C	13.90	14.00	14.10	0.547	0.551	0.555
Cd	17.00	17.20	17.40	0.669	0.677	0.685
E		0.65			0.026	

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